TECHNICAL REPORT ON
ANTI-COINCIDENCE LOGIC UNIT

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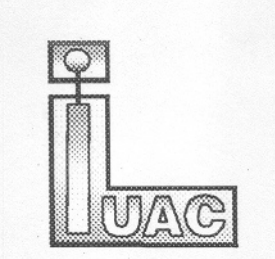

TECHNICAL REPORT

TITLE	**:Technical Report on Anti-Coincidence Logic Unit**
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CATEGORY	**: Instrumentation**
REFERENCE NO	**: NSC/TR/SV/2002-03/28**

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Abstract:

As a part of on going Nuclear Electronics development for INGA project, we have successfully developed a high density Anti-coincidence Logic unit (1) in a daughter card format to use with Clover and ACS detector array. This unit essentially replaces numerous high density NIM modules while conserving NIM bin slots, power and reducing the number of inter connection cables and connectors.

In order to collect datas corresponding to only valid events, the raw timing informations are processed in this unit. This logic unit, receiving raw timing informations from TFA+CFD modules corresponding to clover segments and ACS detectors and further processing is done to generate ADC gating, PUR logic, STOP to TDC, Anti-coincidence logic for Multiplicity. In this report, the operation principles of various circuit blocks and assembly procedures are given in detail.

Acknowledgment

We would like to thank INGA project group at NSC for specifying and evaluating overall timing logic and providing funds for development. We would like to thank engineers from GIP, Ganil, France for their constant support in simulating various circuit blocks and for fruitful discussions. At last, our sincere thanks to Prof. G.K.Mehta Dr.Amit Roy, and Ajith Kumar.B.P, for their constant encouragement and providing the necessary infrastructure inorder to complete this project successfully.

SPECIFICATIONS: ANTI-COINCIDENCE LOGIC UNIT

INPUTS (Internal) **ECL COMPLIMENTARY**

CHANNEL A	CFD 2 μS DEAD TIME CFD 50 nS. width
CHANNEL B	CFD 2 μS DEAD TIME CFD 50 nS. width
CHANNEL C	CFD 2 μS DEAD TIME CFD 50 nS. width
CHANNEL D	CFD 2 μS DEAD TIME CFD 50 nS. width
AC SHIELD	CFD 500 nS. width

MASTER GATE (**MGATE_IN**) TTL (positive) internally pulled up input. Must arrive within 1μS of individual CFD outputs.

OUTPUTS

ANTI-COINCIDENCE (**A_COIN**) **FAST NIM** (Front panel LEMO)
WIDTH 500 nS. (adjusted on BOARD)
After "OR"ing of CFD (50 nS) outputs from CHANNEL A to D "DELAY"ed by ~100 nS. GATED with ACS (500 ηS) for Coincidence and output is generated.

START/STOP(**TDC**) **FAST NIM** (Front panel LEMO)
WIDTH 50 nS
After Coincidence, the signal is DELAYED (200 nS - 800 nS Adjust on BOARD) and output is generated.

MONITOR(**OR**) **Attenuated ECL** (Front panel LEMO)
WIDTH 50 nS
The CFD (50nS) outputs are logic ORed and and delayed ~100 nS

ADC GATEs(**GATE A-D**) **Positive TTL** (Front panel LEMO)
Zo: 10 ohms.
WIDTH 10 μS. Refer to Block diagram. Generated only when Master_Gate is present with 1μS of the input signal.

PUR SUM(**PUR A-D**) **POSITIVE TTL** (Rear panel LEMO)
PUR inspection WIDTH 20 μS
Zo: 10 ohms. It is "OR" of four piled up channels.

DIMENSION 4 " x 0.5" x 3.75" 80 grams. W x H x L

TECHNOLOGY Both through hole and SMD components are used.
Double sided PCB with PTH.

Introduction

In principle, the anti-coincidence logic unit is adopted for replacing numerous high density NIM modules, to conserve power, NIM bin slots and to reduce coaxial cable interconnections. We have designed the anti-coincidence logic unit, which would receive timing signals from clover detector (4 signals) and anti-Compton suppression shield (ACS) in order to reject unqualified events. The same unit provides Pile-Up rejection logic (PUR) outputs to ADC and individual ADC gating signals. This unit also provides "START" signal to TDC.

Principle of Operation

The schematic for Anti-Coincidence Logic (ACL) unit is shown along with block diagram. The inputs to ACL are from TFA+CFD modules correspond to ACS and four clover detector segments. The master gate (TTL) input signal is received from MULTIPLICITY logic unit (MGATE_IN) and for simplicity, MGATE_IN signal is pulled up to supply voltage. The Zero-Cross (Z/C) in CFD is extended for 2μS dead time (Clover only), which in turn provides 50nS wide CFD output. The Z/C of CFD corresponding to ACS is extended to 500nS without any dead time. All the ECL signals are received at ACL unit through complementary ECL (100 ohm) levels.

The CFD outputs are (ECL) applied to OR logic (U11) and GATED (U11 D) with ACS signal. The ORed (U11C) signal is suitably aligned (U12,U13) with ACS signal and Anti-Coincidence (ACOIN) logic signal is generated. The width of resulting signal (A_COIN) is set to 500nSec (U16, C19, R109). The incoming CFD signals are locally level converted to TTL using MC10125 (U2,U7) differential ECL to TTL level converter. These signals are processed further (U4,U5,U9,U10) to generate PUR (Pileup rejection) logic signal, where PUR inspection time is set as 20μSec. They are also suitably gated (U3,U8) with MASTER GATE (TTL), and extended anti-coincidence (U18A ..upto 1μS) (ACOIN_EXT).

A common PUR is generated for ADC by ORing (U17) individual PUR logic signals. The fast NIM (F-NIM) ACOIN signal is level converted with fast inverting

amplifier AD 8011 (U19,U20). The Anti-coincidence logic ouput is used to derive "STOP" signal (F/NIM) for TDC with internally adjustable delay upto 800nS. Fast differential amplifiers are used for level converting ECL signal to F/NIM signal.

The entire circuit is assembled on 4" x 3.5" size double sided glass epoxy with 0.6mm PTH, both through hole and surface mount components are used. The width and delay adjusting potentiometers are assembled and can be accessed on board for settings as desired. The decoupling ceramic and tantalum capacitors are liberally used. The required supply voltages ±5.2V is drawn through 1A diodes from ±6V lines. The -2V supply voltage is generated in Mother board.

Assembly Procedure

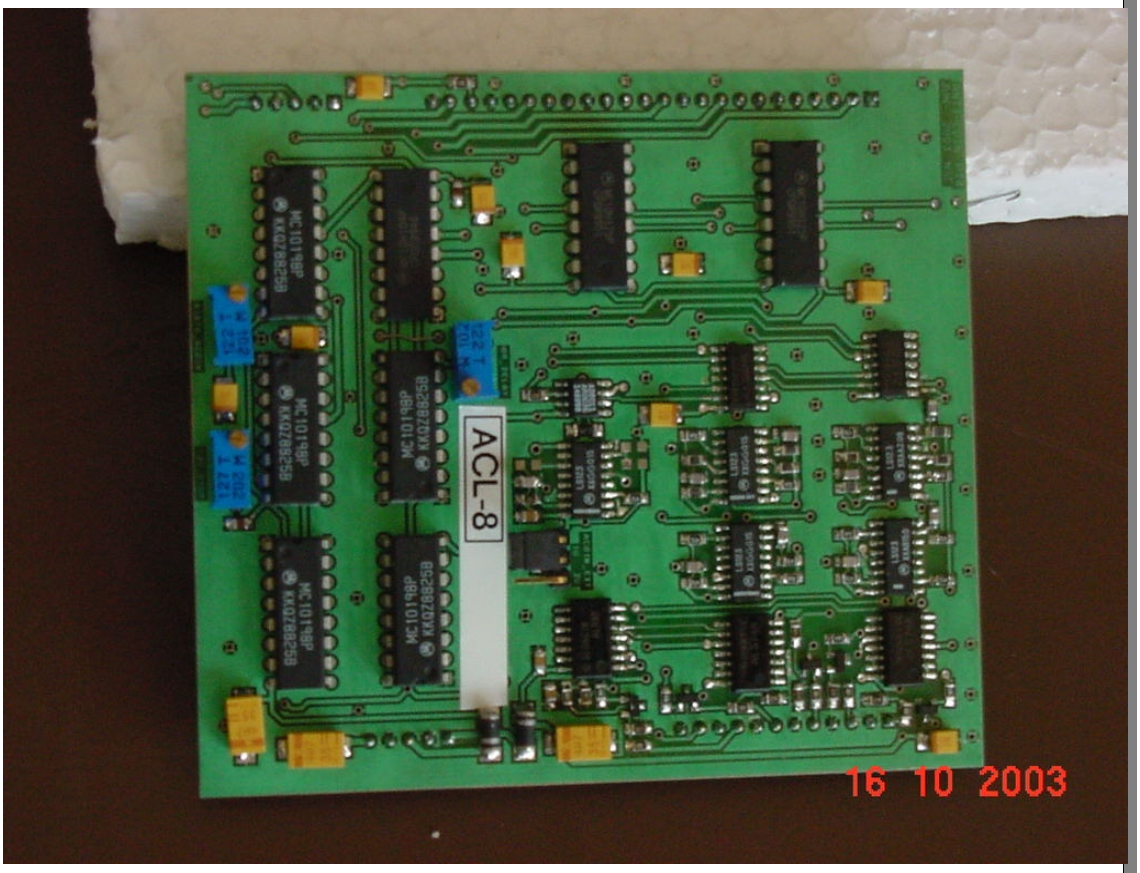
The currently (ANTI-COIN PT-3) available PCB is of glass epoxy, double sided with 0.6mm drill PTH having dimension of 4" x 3.75". It is recommended to have solder mask and silk screen printed on both sides for easy assembly

The PCB shall be checked with magnifiers and multimeter for any unwanted connections and PTHs. Then components shall be soldered in a orderly manner, to start with all low profile chip resistors and capacitors. It is essential to check the impedance between various nodes after soldering resistors, capacitors and inductors. Active components like diodes, transistors and ICS are soldered thereafter. At last tantalum capacitors, connectors, jumpers and any non-SMT devices. All PCBs shall be marked distinctly with unique number for any future references.

References:

1. Electronics for INGA at NSC by Dr.R.K.Bhowmik
2. MECL data book, M/s.ONSEMI, //www.onsemi.com/
3. TTL data book, M/s.ONSEMI, //www.onsemi.com/

Fig: Photo of ACL Unit



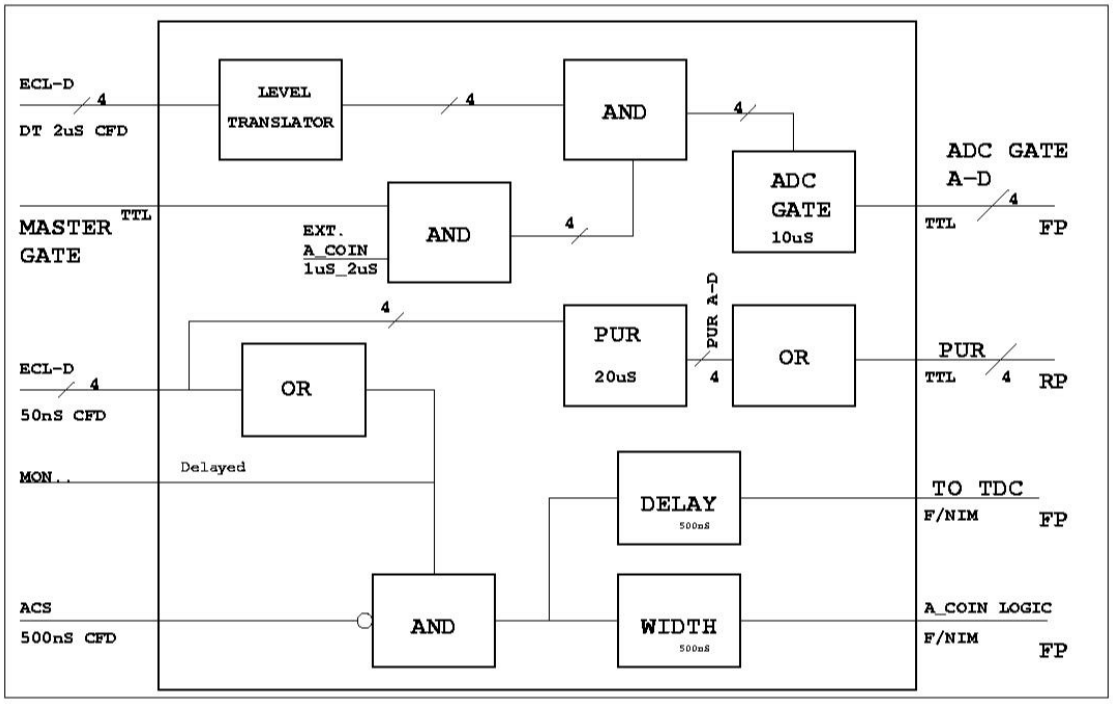


Fig: Photo of Typical ADC Gate Derived from ACL Unit