ON THE DEVELOPMENT OF 30 kVA, 430 Hz SINE WAVE INVERTER FOR DC ACCELERATOR APPLICATION

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Abstract

A 30 kVA, 430 Hz sine wave inverter has been developed based on dual half-bridge operating with sinusoidal PWM with unipolar switching at 20 kHz. The chosen scheme is free from the shoot-through failure and zero-cross-over distortion. The inverter is compact and has been used to carry out low-voltage (up to 200 kV) functional testing of a 2.5 MeV, 100 kW ELV-type DC accelerator at RRCAT.

INTRODUCTION

The high-power ELV-type electron accelerators are widely used in industrial and research applications. The scheme for generating high voltage in these machines is based on air-core, multi-secondary step-up transformer. Each secondary has voltage doubler rectifier and filter, the outputs of which are connected in series to generate the high voltage. As opposed to the conventional transformer, the air-core transformer has large leakage inductance and small magnetizing inductance. The air-core transformer has poor regulation and draws a large reactive power from the source feeding the primary winding. Suitable compensation network (CN) [1] is therefore employed to minimize these undesirable effects. Input port of the CN is excited with a sine wave ac voltage source. This paper describes the development of 30 kVA, 430 Hz inverter (175 V and 175 A rms) developed for this application.

THE DUAL HALF-BRIDGE INVERTER

As opposed to full-bridge or half-bridge voltage source inverter circuits, the dual half-bridge inverter [2] operating with sinusoidal PWM with unipolar switching is chosen for developing the sine wave inverter for the present applications due to following merits:

- Simple scheme for four-quadrant operation
- No shoot-through problem improving reliability.
- High frequency ripple at the input and output of the inverter stage is low and ripple frequency is double the switching frequency, thereby reducing the filtering requirements.
- No zero cross-over distortion due to perfect ripple cancellation at 0.5 duty cycle.

Schematic diagram of the inverter is shown in Fig. 1. Three-phase ac mains is rectified and filtered using diode bridge rectifier and LC filter (L_{dc}-C_{dc}). The filter capacitors are split and the center point is used as the return of the following inverter stage. The inverting stage uses two active switches (IGBTs S_1, S_2) and two diodes (D_1, D_2), for which two half-bridge IGBT modules

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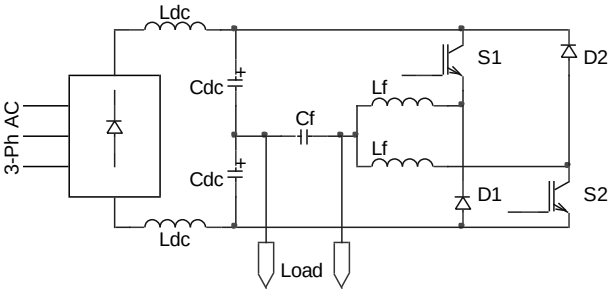

Figure 2: Schematic diagram of the inverter

SKM400GB128D have been used. High-frequency content (40 kHz and multiples) in output sinusoidal voltage waveform is filtered using output filter L_f- C_f.

DESIGN CONSIDERATIONS

Complete steady-state and small-signal analysis of dual half-bridge inverter has been performed to predict various voltage/current waveforms, derive closed-form expressions for their peak, rms and average values and to find out control-to-output transfer function. Instantaneous output voltage is given by $v_o(t) = V_{dc}(d(t) - 1)$, wherein V_{dc} is dc voltage across capacitor C_{dc} and $d(t)$ is instantaneous duty cycle of S_1. Thus, by programming $d(t)$ in sinusoidal fashion, sine wave output voltage can be obtained. It has been observed that the value of L_f has profound effect on current ratings of various components and the size of L_f itself. For instance, defining, critical filter inductance as $L_c = 2R_L(1 - D)/F_s$ (R_L being load resistance and F_s being switching frequency) expressions for peak, average and rms current ratings (normalized to output current) of switch S_1 are derived as $I_{s1,pk} = 1 + \gamma$, $I_{s1,avg} = D(1 + \gamma)$, $I_{s1,rms} = \sqrt{D/3}\sqrt{3 + 3\gamma + \gamma^2}$, wherein $\gamma = L_c / L_f$ Figure 2 illustrates effect of L_f on various current ratings in a typical case.

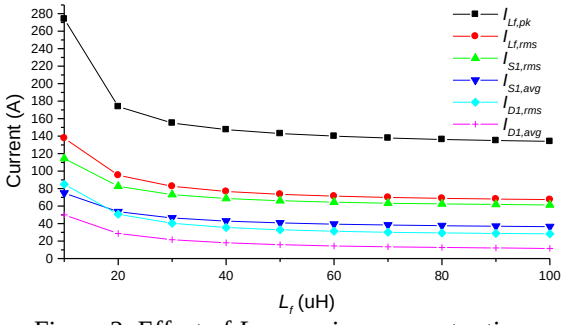

Figure 2: Effect of L_f on various current ratings.

Control-to-output transfer function is derived as $G(s) = \hat{v}_o(s)/\hat{d}(s) = 2V_{dc}/\left(L_f C_f/2\, s^2 + L_f/2R_L\, s + 1\right)$. It can be observed that two filter inductors effectively act in parallel thereby improving the dynamic response of the converter. Fig. 3 shows the plots of this transfer function in a typical case and its comparison with the ones obtained from cycle-by-cycle simulation.

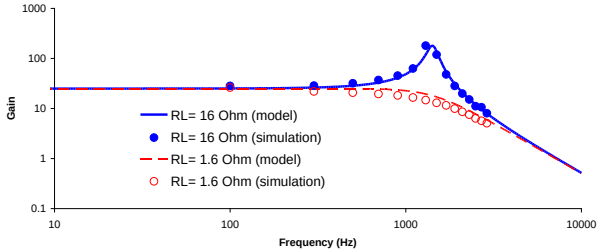

Figure 3: Plots of control-to-output transfer function.

PRACTICAL ISSUES AND RESULTS

Peak voltage/current stress during switching transitions and switching loss are important issues in switch-mode converters. Apart from theoretical design of stress and loss relieving circuits (snubbers and soft-switching techniques), their practical implementation, circuit layout, choice of components and non-ideal behaviour of snubber components are very important factors in achieving intended functionality. In the reported inverter, RCD turn-off snubber is placed across IGBTs to reduce the turn-off switching loss. Similarly, saturable inductor turn-on snubber along with RCD over-voltage clamp is placed in the dc bus to reduce turn-on switching loss, to limit the diode reverse recovery current and to limit the over-voltage spikes across the devices. It has been shown [3] that stray inductance of the RCD turn-off snubber path and forward-recovery voltage of the snubber diodes play vital role in snubbing effectiveness. Figure 4(a) shows voltage across IGBT during turn-off when these factors are not optimized. Resulting initial peak in the voltage waveforms increases switching losses. Improved waveform obtained using low-forward-recovery snubber diode and optimized assembly is shown in Fig. 4(b). Linear inductors used to limit the diode reverse recovery current result in high stored energy and bulky RCD over-voltage clamp. Therefore saturable inductors are preferred, which in turn suffer from high core losses. Heat dissipation in conventional core structures (e.g. toroids) is limited due to limited surface area increasing their temperature. A saturable inductor is therefore developed using planar core which has large surface area to volume ratio facilitating heat removal, which is further enhanced by mounting the core on water-cooled heatsink near IGBT modules. Standard planar E-type core was modified by grinding its central leg to suit the present application as shown in Fig. 5. The value of saturated inductance is also important to avoid current peaks, ringing and EMI as shown by waveforms of Fig. 4(c) and (d).

Figure 6 shows the photograph of the inverter having overall dimensions are 0.7m(W) X 0.9m(D) X 8U(H).

The inverter has been used to carry out low-voltage (up to 200 kV) functional testing of a 2.5 MeV, 100 kW ELV-type DC accelerator at RRCAT.

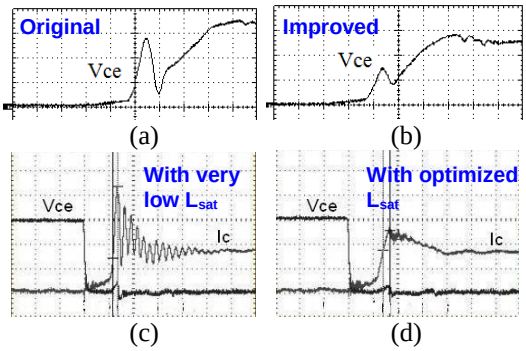

Figure 4: (a), (b) IGBT voltage waveform at turn-off. (c), (d) IGBT voltage and current waveforms at turn-on.

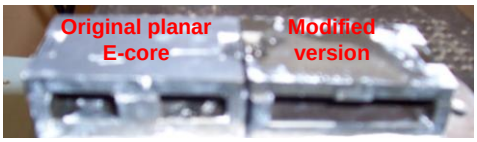

Figure 5: Planar core used for saturable inductor.

Figure 6: Photograph of the inverter.

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