CHARACTERIZATION OF FPGA BASED LOW-LEVEL RF BOARD

J. A. Gore#, S.G. Kulkarni, P. V. Bhagwat, A. K. Gupta, R. K. Choudhury,
NPD, BARC, Mumbai 400 085

Abstract

As part of the ECR injector project, a Field Programmable Gate Array (FPGA) based board for Low Level RF (LLRF) applications has been designed and developed. Characterization of the developed board is essential to ensure that the board can be used to develop and test LLRF control applications. This paper describes the implementation of the algorithms used to characterize the board. Parameters like Signal-to-noise distortion ratio (SINAD), Spurious Free Dynamic Range (SFDR), Effective number of bits (ENOB), Differential and Integral nonlinearity (DNL & INL), and Data transfer throughput have been measured and are used to characterize the board. The test set-up (consisting of an RF source, an in-house designed digitally programmable band pass filter) used to measure these parameters is described and the results obtained using the same are reported in this paper.

INTRODUCTION

A heavy ion RFQ (75 MHz) is being developed at PAF, BARC-TIFR. It is designed to accelerate ion beam from 10 keV/u to 575 keV/u over a vane length of 4.62 m. A 1.42 m prototype RFQ with 1.34 m of modulated vanes is fabricated to study aspects related to RF properties, power coupling methods and RF control. Amplitude and phase control of the electromagnetic fields of the RFQ is essential to ensure a stable beam. To achieve this, a FPGA based board LLRF control board has been designed. Characterization of this board is essential to ensure that it can be used for controlling the RF fields of the RFQ.

The paper is categorised into three sections. The first section describes briefly the board details and features. The second describes and reports the parameters related to the characterization of the board and the third concludes and briefly presents current status of the board.

BOARD DETAILS

The developed board shown in figure 1 is designed to function in a stand-alone mode and has on-board Virtex-5 FPGA. Data acquisition is achieved through four on-board, 14bits, 125 MSPS analog input and output channels. For data storage a 2GB DDR2 RAM has been provided. USB 2.0 and Ethernet ports are included on-board to ensure data transfer to the PC. To enable high speed data transfer 06 rocket-IO based SFP connectors have also been provided. Apart from this 16 user IOs ensure that the board functionality can be enhanced.

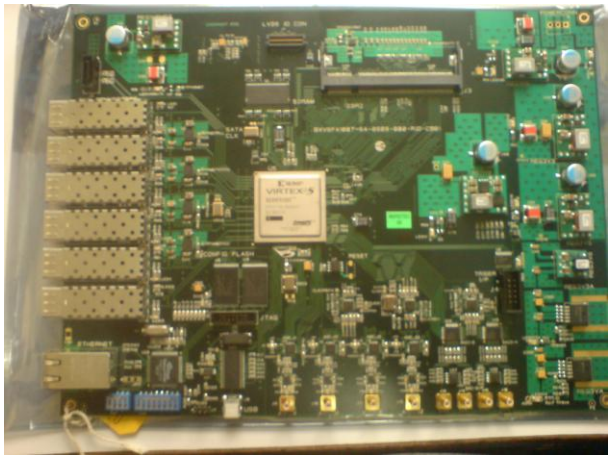


Figure 1: LLRF board

BOARD CHARACTERIZATION

The board has been characterized by measuring SINAD, SFDR, ENOB, DNL and INL. The first three parameters have been measured using the FFT method. The last two viz. DNL and INL have been measured using the histogram method. For both the methods a sine wave input was used. The ADC was slightly overdriven. The sine wave input was obtained from a stable sine wave source (Stanford Research Systems Model DS345). This was filtered to remove harmonics using a bandpass filter developed in-house. The centre frequency of the filter is digitally programmable. Data from the ADC was transferred to the PC through the USB port. The parameters were computed off-line. The test set-up is shown in figure 2.

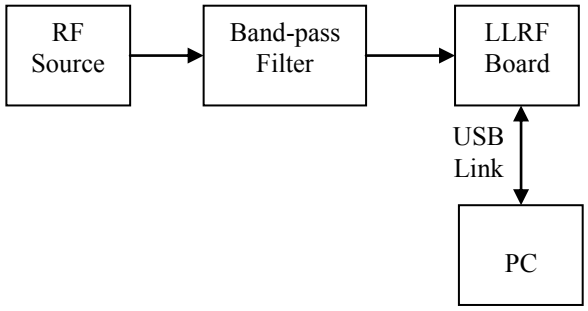


Figure 2: Test Set-up

Bandpass Filter

A dual section biquad filter in a band pass mode is used to remove the harmonic content from the RF source. The centre frequency is digitally programmable from 1 MHz to 10 MHz. The minimum quality factor obtained was 900. The schematic of one filter section is shown in figure 3. The filter is made digitally programmable by choosing a digitally programmable resistance.

#jagore@tifr.res.in

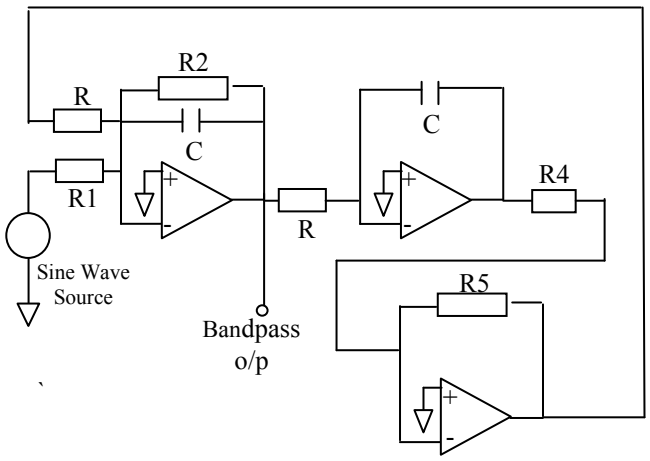


Figure 3: Bandpass filter

Measurement of parameters

As mentioned before the SINAD, SFDR and ENOB is measured using the FFT method. For this, a sine wave signal is applied to the filter input and the output of the filter is digitized and acquired by the PC through the USB link. The FFT of the acquired input is obtained and from this spectrum the parameters are calculated. The equations used for calculating the parameters are as follows:

$$SNR = \frac{S}{NoiseFloor}$$

$$THD = \sqrt{(10^{-v2/20})^2 + ... + (10^{-v6/20})^2}$$

$$SINAD = 20\log_{10}\sqrt{(10^{-SNR/20})^2 + (10^{-THD/20})^2}$$

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

The Noise Floor level is first measured with a 0V signal applied to the filter. The ENOB was measured from 1 MHz to 10 MHz. The centre frequency of the filter was set at the input signal frequency. The worst case ENOB of 11.47 bits was observed at 10 MHz. Figure 4 shows the variation of ENOB as a function of frequency. The DNL and INL were measured using the histogram test procedure [1]. A total of 02 GB samples were collected to calculate the DNL and INL. The DNL and INL plots are shown in figure 5. Table 1 shows the measured parameters at 10 MHz input frequency.

Table 1: Measured parameters at 10 MHz input frequency

SINAD	70.809 dB
ENOB	11.47 bits
SFDR	72.267 dB
DNLmax	+/- 0.5 lsb
INLmax	+/- 0.76 lsb
THD(Tot. Harmonic Distortion)	48.687 dB
SNR	70.782 dB
Throughput (1 MB data)	3.22 MB/sec (Approx)

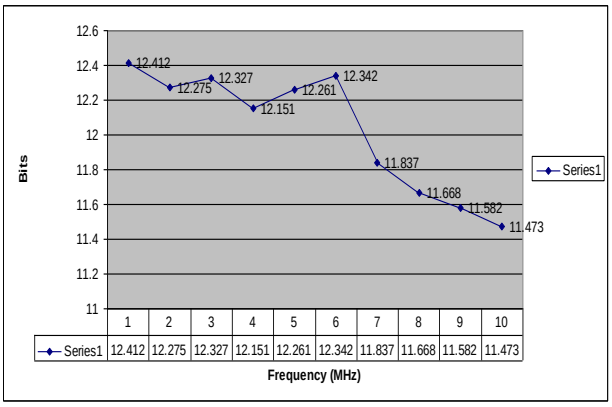
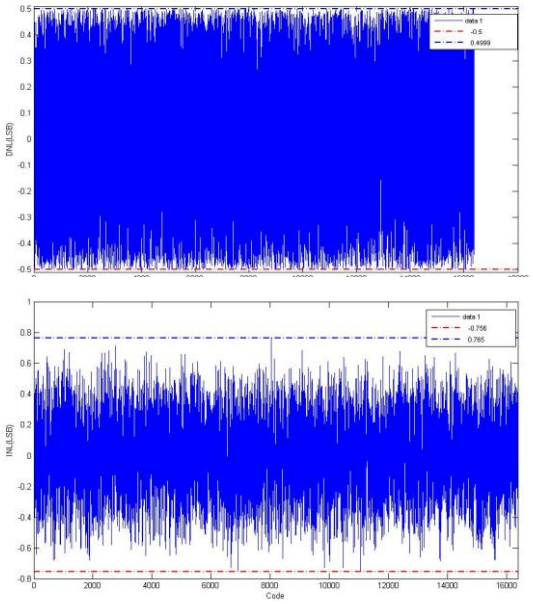


Figure 4: Variation of ENOB with input signal frequency

Figure 5: DNL and INL plots



CONCLUSION

Characterization of the LLRF board is almost complete. The reported parameters have been measured at the maximum ADC sampling frequency of 125 MSPS.

Jitter measurements are on-going. Characterization of the board with all 04 analog inputs simultaneously acquiring data is being planned.

At present the board has been used successfully to develop the I/Q demodulator scheme [2].

REFERENCES

[1] Walter Kester, Chapter 5: Testing ADC, Analog Devices.

[2] S. G. Kulkarni et al., Design and development of digital I/Q modulator, InPAC-2011, February 15-18, IUAC, New Delhi.