TECHNICAL REPORT

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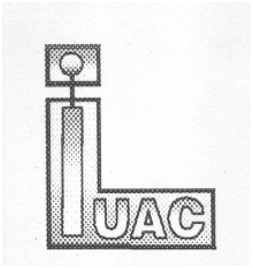

TECHNICAL REPORT ON

INGA-LEPS ELECTRONICS MODULE

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TECHNICAL REPORT ON

INGA-LEPS ELECTRONICS MODULE

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Abstract:

A NIM module containing Shaping amplifiers, TFAs, CFDs and logic circuitry for processing signals from a LEPS (Low Energy Photon Spectrometer) detector with optional Anti Compton Shield (ACS) has been developed. The circuits are realised in High density daughter card form using SMD components, while keeping the features and specifications at par with commercially available modules. The present module is essentially a modified version of Clover electronics module of INGA ie. segmented clover HPGe type detector, wherein the main shaping amplifier and Timing Filter Amplifier gain are altered for LEPS type detector, which have relatively lower energy sensitive range. The module is tested with LEPS detector at VECC, Kolkata for the suitability with INGA setup. The same are mass produced and delivered for INGA applications at IUAC.

Acknowledgment

We would like to thank Mrs. Sarmista Mukherjee of VECC and her colleagues for testing the module along with commercial electronic modules and reporting the test results. Our sincere thanks to Dr. Amit Roy, Ajith Kumar B.P for their constant encouragement and providing the necessary infrastructure in order to complete this project successfully. Special thanks to all those provided valuable feedback in order to improve upon previous version(s). We also thank M/s. ANCOMP for their help in providing good quality PCBs, and
M/s. Sankar System for component assembly.

Introduction

The experimental facility like INGA consists of a large number of HPGe detectors (4 segment clover type) and few numbers of LEPS detector. LEPS detector are identical to HPGe Clover detector in geometry but not sorrounded by ACS detector. These detectors are efficient for low energy gamma rays. To process signals from LEPS detector, each channel requires a high quality Spectroscopy amplifier, Timing Filter Amplifier (TFA) and Constant Fraction Discriminator (CFD) and associated Logic circuits. Typical commercial electronic setup would require a large number of modules which occupy large area, interconnecting cables and connectors. The NIM module developed at IUAC contains entire front end electronics to process signals from a LEPS detector sorrounded by optional anti-Compton shield#. The content of this double width NIM module is shown in fig 1.

#: Usually LEPS is not mounteded with ACS detector.

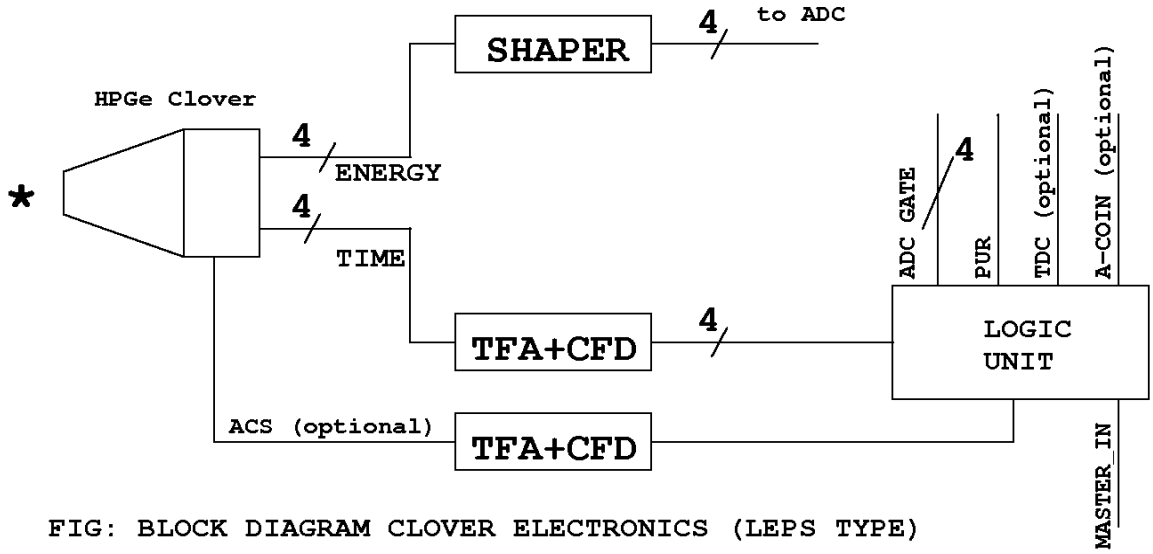


FIG: BLOCK DIAGRAM CLOVER ELECTRONICS (LEPS TYPE)

The high resolution spectroscopy amplifiers have fixed 3μs shaping constant and 2 fixed gain settings (0.3 & 0.6 MeV respectively) which are jumper selectable. The DC baseline is stabilized with Gated BLR, while P/Z and BLR (manual) threshold adjustments can be remotely voltage controlled. The unipolar output has the dynamic range of 8 volts across 50 ohms.

Four TFAs with fixed time constants and gain settings are provided for processing TIMING signals from LEPS detector. The TFA is designed with single CFA gain stage and baseline is stabilized with twin diode restorer and high input impedance buffer. These amplifiers have rise time of better than 10 ns across their dynamic range of ±2.5 volts across

100 ohms. The CF Discriminator with amplitude and rise time compensation (ARC) is realized with fixed delay of 25 ns and fraction of 0.3. The Lower Level Threshold, WALK adjustment and Monitoring are possible on front panel. The CFD outputs from the individual LEPS elements with width of 50 ns and dead time of ~2 μs are set internally.

Anti-Compton shield signal received from ACS Preamplifier is processed with identical TFA + CFD as mentioned above but without dead time. The raw timing logic signals received from CFDs from LEPS detector and optional ACS detector are further processed to affect Anti-coincidence. The TFA and CFD outputs from the optional ACS are available on the panel for ease of adjustment. The logic functions performed in Anti Coincidence Logic unit are Pileup Rejection (PUR), generation of individual ADC GATE (GATE), Anti-Coincidence (ACOIN) output and Delayed STOP signal for Time to Digital converter (TDC). All these logic outputs are buffered and available in standard logic levels (TTL, F_NIM) on the panel.

Principle of Operations

The INGA-LEPS Electronics Module is a double width NIM module that contains a mother board, where individual blocks in daughter card form are inserted. The DC supply lines are filtered with PI filter section, and a negative 2V zener regulated supply is generated. The rear panel receives the inputs like "ENERGY" and "TIME" signals from Preamplifier through Lemo (00 series) connectors. The Front panel provides the various monitoring points like P/Z Mon., BUSY, WALK_MON, Energy OUT, ADC GATE and other Logic related signals (TDC STOP, ACOIN..) through Lemo connectors and manual control of various adjustment like P/Z Adj., BLR Threshold adj., WALK adj., LLTH adj., through multi turn potentiometers. The TFA (optional ACS) and CFD (F_NIM) outputs corresponding to LEPS elements are provided for monitoring. The panel layout can be seen in attached photograph or drawing.

The high frequency signal layout techniques are widely used for reduction of ground loop related and pick-up problems in the motherboard. RG178C/U coaxial cable is used for interconnection along with ground cap with Lemo-00 series connectors. Typical cable lengths used for various interconnections inside the module are listed here. The Timing signals from TFA+CFD block are routed through 100 ohm differential ECLlines for further processing. The detailed operation principles of various blocks briefed here can be obtained from

individual technical reports prepared by the Electronics Laboratory.

The technical specifications, photographs, representative signals seen on CRO of Shaping Amplifier, TFA+CFD, ACOIN LOGIC UNIT are attached for references.

Temperature Measurement:

The temperature measurement inside this module is accomplished by the Voltage reference chip **ADR03**, in order to measure the temperature inside the module and correlate the performances of various sub-circuits built in. This is required, due to presence of large number of high density electronics module in electronics singal processing area dissipating heat.

The TEMP pin readily available in this chip is accessed through a current protection resistor on the rear panel, and typical values measured with respect to analog ground of the NIM bin are as follows.

Temperature	***Cooling***	***Voltage measured***	***Observation***	***Observation***	***Time taken***
25 ºC	No	552mV	LLTH:-200mV	WALK_ADJ..	0 Sec
52ºC	No	605mV	LLTH:-200mV	Shifted UP (+)	50 Min.
36ºC	Yes	573mV	LLTH:-200mV	Original value	15min.

The instrument cooling fan is operated in order to maintain the near room temperature for a temperature stable operation. Where, the ADR03 along with amplifier circuits (LT1361) provides an excellent thermal stable reference supplies (dual polarity) for LLTH, WALK ADJ. Settings, and other voltage controlled parameters such as P/Z Adj., BLR reference settings.

Indication of ADC 'GATE':

In order to visualize the presence and rate of ADC 'GATE' signals, additional circuit has been incorporated on the motherboard. The ADC GATE signals generated by ACLogic card is utilised to trigger a monostable multi vibrator circuit to enable the LED on the front panel.

SPECIFICATIONS

LEPS ELECTRONICS MODULE

ENERGY 4 SHAPERS with 3 µS Shaping constant and fixed gain for
0.3* MeV / 0.6MeV
*** Default** selection, Selected with 2 jumpers on PCB.
Input and Outputs are accessed through LEMO connectors on Rear and Front panel respectively.

Controls for P/Z adjustment and BLR Threshold on Front panel.

Monitoring of **BUSY** and CLAMPED E_OUT (**P/Z MON**) possible through Front panel LEMO connectors.

TIMING 5 Timing Filter Amplifiers and Constant Fraction Discriminators for 4 LEPS detectors and optional ACS respectively.

Timing Inputs are through Rear panel LEMO connectors.

WALK ADJUST, LLTH ADJUST, WALK MONITOR#, LLTH MONITOR on front panel.

TFA (attenuated) signal monitor for optional ACS is provided on front panel.

CFD outputs (F_NIM / 50nS & 500nS (optional ACS)) are available on rear panel.

PUR reject (TTL) available with 20uS monitoring period available on rear panel

ANTI-COINCIDENCE LOGIC UNIT

Accepts all required timing informations in ECL complementary logic levels from TFA+CFD units. The outputs and Monitors are provided on front panel through LEMO connectors.

Presence of ADC '**GATE**' signal is indicated with LED on front panel.

The **ACL**ogic DELAY and WIDTH adjustments are possible on PCB.

MASTER GATE input (MGATE_IN) is TTL logic (positive) with "pull up" resistor.

TEMPERATURE

Measurement of module inside temperature is possible through rear side '**TEMP**' test point. Ref: @ **25˚C, 550mV** with Temp. coefficient of **~2mV/˚C**

CABINET Double width NIM module

RECOMMANDATION

To assemble 4 Nos. of this module in a standard 200 watts NIM Crate with forced air cooling from bottom of the NIM crate at ambient temperature of 25 deg.C, 50%RH.

Power Consumption: +/-6V@ 0.7A/1.9A, +/-12V@ 0.3A/0.3mA, +24V@0.03A

SPECIFICATIONS
SPECTROSCOPY AMPILIFIER*

Input Impedance	~1000 ohm
Pole/Zero adj.	Input pulse having decay time about 50μSec ± 5% can be corrected through potentiometer (FP) or remote controlled through DAC. Input impedance: 1K Input voltage not to exceed ± 1Volt.
Shaping	
Type & Time	~3 μSec. Fixed, Active integration (4^{th} order) Quasi Gaussian having peaking time of 2.4τs.
Input signal*	-200mV/MeV is expected to generate +10 Volts at the output for 2 gain settings. Not to exceed ±10V.
Gain	0.3MeV / 0.6MeV for +10V output. Jumper selection on board. Default is 0.3 MeV.
BLR threshold	Manual baseline restorer threshold is set through Potentiometer(FP) or remotely. Range is 0 to 600mV when provided. Impedance is 1k. Control voltage not to exceed ±10V
Output	Unipolar, Gated BLR DC restored. Width :~20μSec. Impedance 50 ohm
BUSY	A TTL negative logic pulse for the duration of presence of output pulse exceeds BLR threshold. Impedance: 10 ohm.
PUR (optional)	Pile up reject signal is a TTL positive logic signal, with pileup inspection interval of 20μSec. Impedance: 10 ohms.
Power required*	+/-6V, 0.04A/0.02A +/-12V 0.04A/0.03A +24V/ 0.005A
Size & Weight	W x H x L : 1.75"x0.5"x 4", 30 grams.
Technology	Double sided PCB with PTH and SMD components are used.

PERFORMANCES:

Integral non-linearity: ± 80 eV for ^{60}Co spectrum.
Stability: With ^{60}Co, no significant shift observed at 6 kcps in 55 hours.
Resolution: ~1KeV at ^{252}Eu low energy peaks < 121 KeV

SPECIFICATIONS
TIMING FILTER AMPLIFIER*

INPUT IMPEDANCE	50 ohms.
GAIN(fixed)*	~65 (LEPS_Ge)/15 (optional ACS) The input of -200mV/MeV is expected from Preamplifier.
OUTPUT AMPLITUDE	0 to ±2.5V into 50 ohm cable and load.
OUTPUT IMPEDANCE	~10 Ohm
RISE TIME	Better than 10nSec. With no additional integration across dynamic range.
Baseline Correction	Twin diode restorer used.
POLE/ZERO ADJ.*	P/Z internally corrected for 50μS (±5%) decay time internally.
DIFFERENTIATION	200nS (C1 X R12)
INTEGRATION	10nS. (R4 X Cx)

* For optional ACS, the P/Z network is wired for 400nS internally to match the decay time of BGO phosphor.

SPECIFICATIONS
CONSTANT FRACTION DISCRIMINATOR*

INPUT SIGNAL	Negative pulses accepted unto -5V
THRESHOLD RANGE (LLTH)	+60mV to -200mV (actual) Front panel adjustable.
LLTH MONitor	Measures x10 of actual LLTH set value.
DELAY	Internal, Zo: 100 0hm, 25nSec Fixed.
FRACTION RATIO	: ~ 0.3
WALK ADJUST	Front panel control for exact zero-cross voltage.
WALK MONitor	Front panel LEMO connector for monitoring CF signal.
DEAD TIME	~2 μS. (Fixed)
WIDTH	~50nS.(Fixed)
OUTPUTS	ECL DIFFERENTIAL 2 μS internal. ECL DIFFERENTIAL 50 nS internal. FAST NIM (2 nos.) 50 nS. Rear panel (optional)
IMPEDANCE	100 ohm DIFFERENTIAL ECL 50 ohm FAST NIM
OTHERS	SRT/CFD(Default) selection (Jumper on board)
DIMENSION (WXHXL) & WEIGHT	1.5" x 4" x 0.5", 50 grams
TECHNOLOGY	Both SMD and Through hole components used. Masked PCB 1.6mm/70μM Double sided with PTH.

Note: For optional ACS, the same CFD daughter card is used without any dead time and output having width of 500 ηS.

SPECIFICATIONS: ANTI_COINCIDENCE LOGIC UNIT*

INPUTS (Internal) ECL COMPLIMENTARY (Zo=100)

CHANNEL A	CFD 2 μS DEAD TIME CFD 50 nS. width
CHANNEL B	CFD 2 μS DEAD TIME CFD 50 nS. width
CHANNEL C	CFD 2 μS DEAD TIME CFD 50 nS. width
CHANNEL D	CFD 2 μS DEAD TIME CFD 50 nS width
AC SHIELD	CFD 500 nS width

MASTER GATE (MGATE_IN)

TTL (positive) internally pulled up input.
Must arrive within 1μS/2μS of individual CFD outputs.

OUTPUTS

ANTI-COINCIDENCE **(A_COIN)**
FAST NIM (Front panel LEMO)
WIDTH 500 nS. (adjust on BOARD)
After "OR"ing of CFD (50 ns) outputs from channels A to D "DELAY"ed by ~100 nS. GATED with optional ACS (500 nS) for Coincidence and output is generated.

START/STOP(**TDC**)
FAST NIM (Front panel LEMO)
WIDTH 50 nS
After Coincidence, the signal is DELAYED (200 nS-800 nS Adjusted on BOARD) and output is generated.

MONITOR(**OR**)
F_NIM (Front panel LEMO)
The CFD (50 nS) outputs are logic ORed and Level converted and shaped (100nS).

ADC **GATE**s(GATE A-D)
Positive TTL (Front panel LEMO) LED Indicated.
Zo: 10 ohms. WIDTH 10 μS.
Refer to Block diagram. Generated only when Master_Gate is present within 1μS of the input signal.

PUR SUM(PUR A-D)
POSITIVE TTL (Rear panel LEMO)
PUR inspection WIDTH 20 μS
Zo: 10 ohms. It is "OR" of four piled up channels.

DIMENSION
Double Width NIM Module (DOE)
4 " x 0.5" x 3.75" 80 grams. W x H x L

NOTE: * Refer individual technical report for details.

Operational Procedures

Gain Selection Procedure:

The "Shaper" is designed to work with one of the three different GAIN settings 0.3MeV*/0.6MeV as per user requirement. The GAIN can be selected on the SHAPER daughter card by the procedure given here.

Open the side panel of LEPS Electronics Module

1. Locate the SHAPERS in TOP of Mother Board.
2. Identify JUMPER SOCKETS in extreme right corner facing top. (Ref. Photograph)
3. By plugging 'in' other the jumper will select 0.6MeV.

We suggest the user not to plug out the daughter card for GAIN change, instead use tweezers/sharp nose pliers to plug in/out jumper headers for gain change.

Pole_Zero Adjustment:

The Shaper is designed to work with Eurisys Measures LEPS detectors with preamplifier s having 50μS (±5%) decay time constant. The Pole_Zero adjustment can be done with front panel PZ_Adj. Potentiometer while monitoring corresponding front panel PZ_ Mon. on a CRO. Any major deviation (above ±5%) in decay time can be corrected in Preamplifier card as suggested by the manufacturer.

BLR Adjustment:

The Shaper is designed to have stable zero reference at all specified working conditions. This is achieved by Gated BLR operation. The required threshold level above system noise is fed through front panel BLR adj. potentiometer. This is set while monitoring front panel BUSY (TTL) signal on a CRO for a minimum count rate when no radiation sources are used. It is essential to set proper Pole Zero adjustment for proper functioning of BLR. During above procedures, it is recommended to use corresponding BUSY signal to trigger CRO.

Schematic Diagram

For easy references, a set of circuit diagrams are attached. The circuit diagram of individual blocks can be obtained from Electronics laboratory, IUAC. The entire mother board is mounted on side rails of a double width NIM module. The individual blocks are assembled in daughter card form and plugged into low profile machine trimmed sockets. The front panel trimmer potentiometers (3006P) are hood mounted. The series pass regulator transistor is electrically isolated and mounted on rear panel for heat sinking.

Assembly Procedure

The currently (MOTHERBRD, April 2006, Rev:3) available PCB is of glass epoxy, double sided with 0.6mm drill PTH having dimension of 7.25" x 8.5". It is recommended to have solder mask and silk screen printed on both sides for easy assembly as well to protect it from solder bridges etc.,. Use of 0.2mm sharp solder tip, IC solder tips are recommended in order to solder narrowly spaced SMT devices. SMT devices shall be picked only by fine quality tweezers. While soldering a magnifier x5 (large) and x12 (eye piece) is used to assure the soldering. It is essential to use solder cleaning liquid/thinner with cotton swab to remove dust attracting solder paste.

The PCB shall be checked with magnifiers and multimeter for any unwanted connections and PTHs. Then components shall be soldered in a orderly manner, to start with all low profile chip resistors and capacitors. It is essential to check the impedance between various nodes before and after soldering resistors, capacitors and inductors. Active components like diodes, transistors and ICS are soldered thereafter. Atlast tantalum capacitors, connectors, jumpers and any non-SMT devices. All PCBs shall be marked distinctly with unique number for any future references. The Series pass transistor is mounted in conventional way with heat sink kit.

Reference:

1. Electronics for INGA at NSC by Dr.R.K.Bhowmik

Assembly Procedure:

Check for any solder bridge with Magnifier lamp + magnifier eyepiece (x10/x12) as well as with multimeter. Known solder bridges in this PCB are listed in this manual. Apply thin flux for good solder connection (No clean solder flux recommended). Assemble the pins first carefully flush mounted, with great care to avoid any solder bridges and excess solder. Assemble the resistors and capacitors 0805 foot print and SOT123 active parts like diodes. Capacitors (polarised) would be followed with RFCoils wound as per instructions given in schematic.

Check again with magnifier for any solder bridges and shorts with multimeter. Clean the PCB with good Pcb cleaner/thinner and cotton for any excess Flux which attracts dust during long operation. Check the mother board with DC power supply and multimeter for working of M2V supply line and power supply distribution to all daughter cards.

Preparation of Cabinet:

The double width cabinet of NIM standard is used as housing for this module. The mother board Pcb shall be placed on the rails inside the cabinet for proper sizing before fixing it. Excess projection of PCB shall be removed with "Rough File" before component assembly. The front panel and back panel punch details are given in this manual and punching shall be done with great to avoid wastage of cabinet assembly. The screen printing can be done after punching of the panels. The sample screen print schematic is also attached here. The PCB is secured on the side rails with four numbers of 4-40 size 1/4inch pan head screws on tapped holes.

Wiring:

The standard length of 3 core flat wire and RG178C/U used for interconnections inside the module are listed for easy assembly. Good hand tools and neat assembly procedure shall be followed for any maintenance free operations. The connections involving coaxial cables shall be done first and followed by potentiometer connections. Confirm the wiring also with good quality continuity checker (multimeter). While mounting the LEMO connectors and potentiometers, avoid any scratch to front and rear panels, and use standard tools for quality finishing. The wiring orientations shall be checked while powering the unit with daughter cards and necessary wiring correction shall be done in case of any reversal.

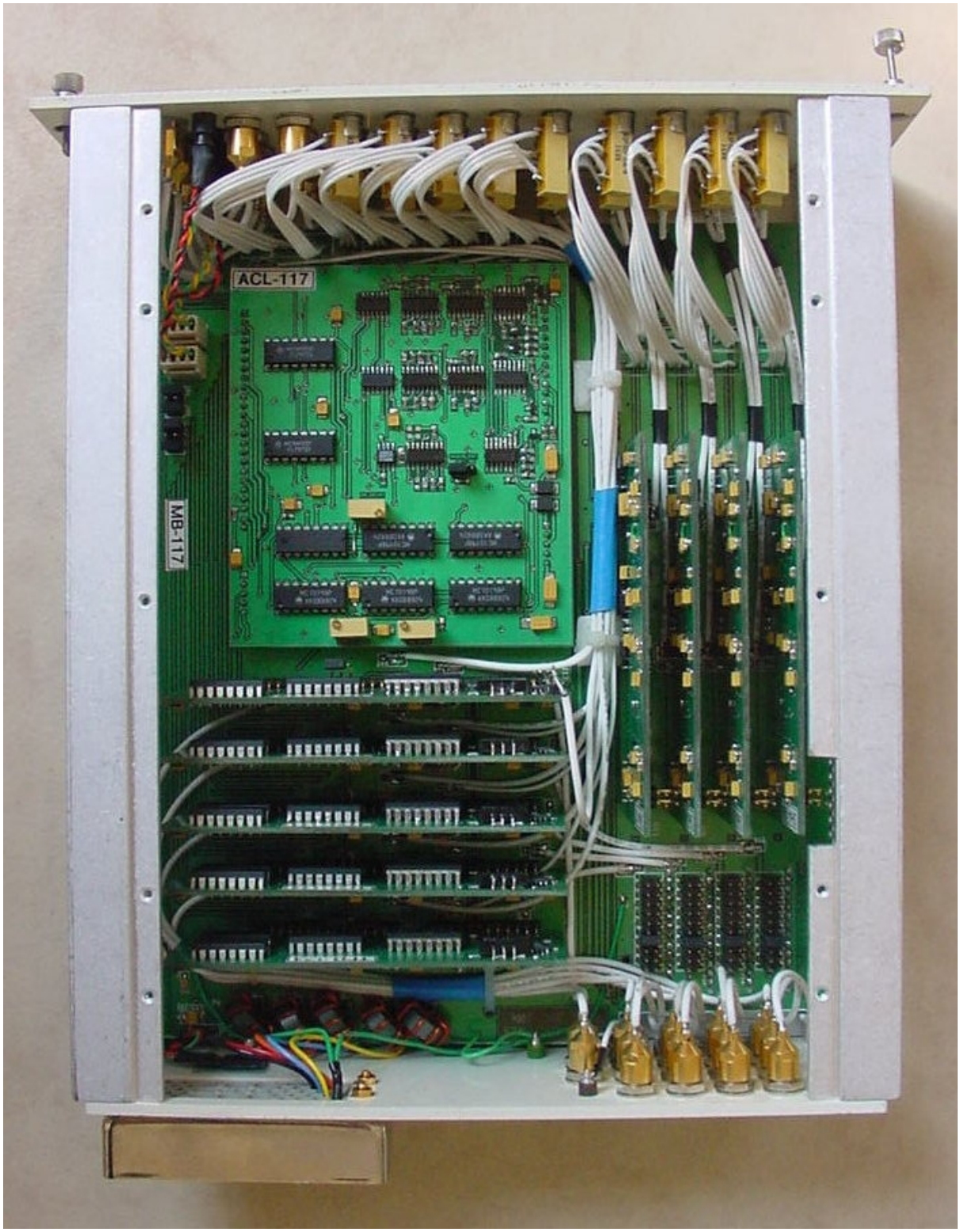


Fig: Inside view of the INGA_LEPS Electronics Module

Fig: Front & Rear View of INGA_LEPS Electronics Module

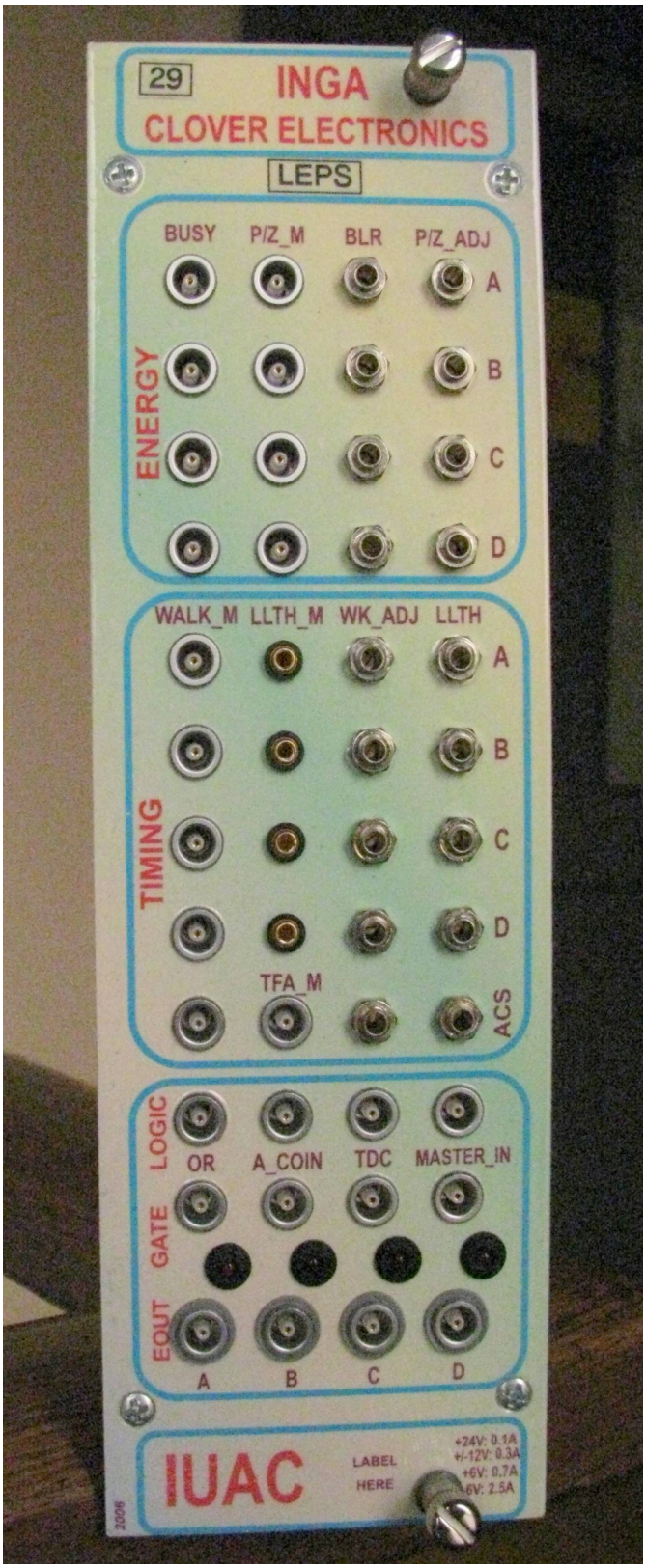
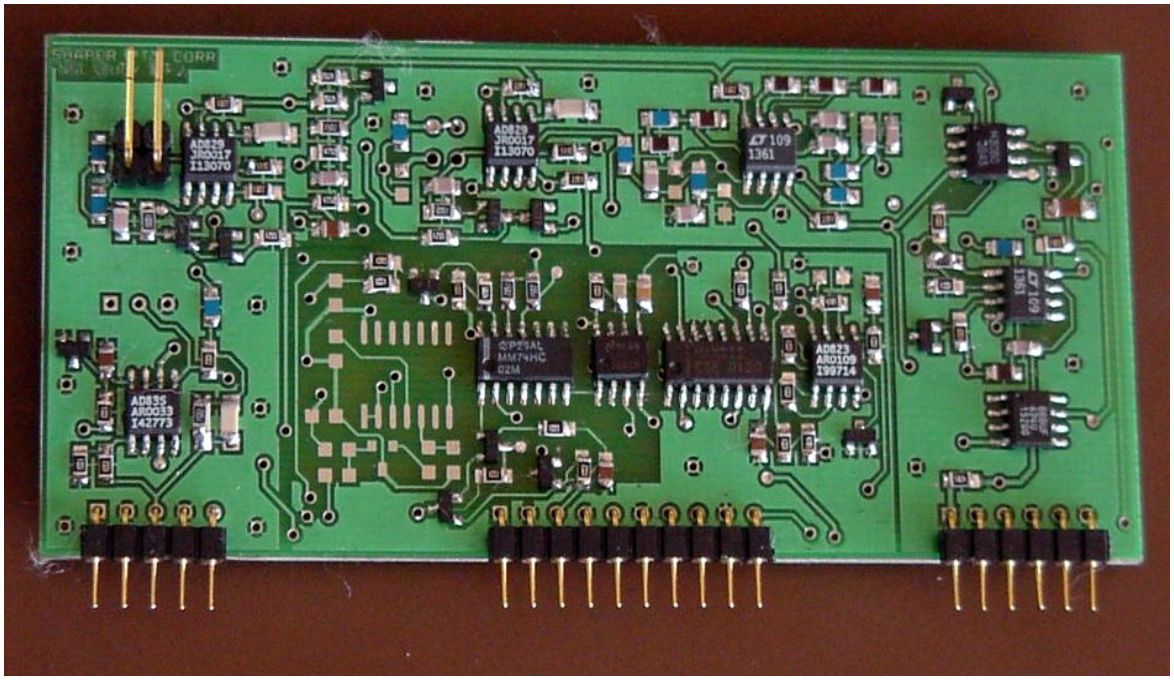


Fig: Shaper card with typical signals monitored



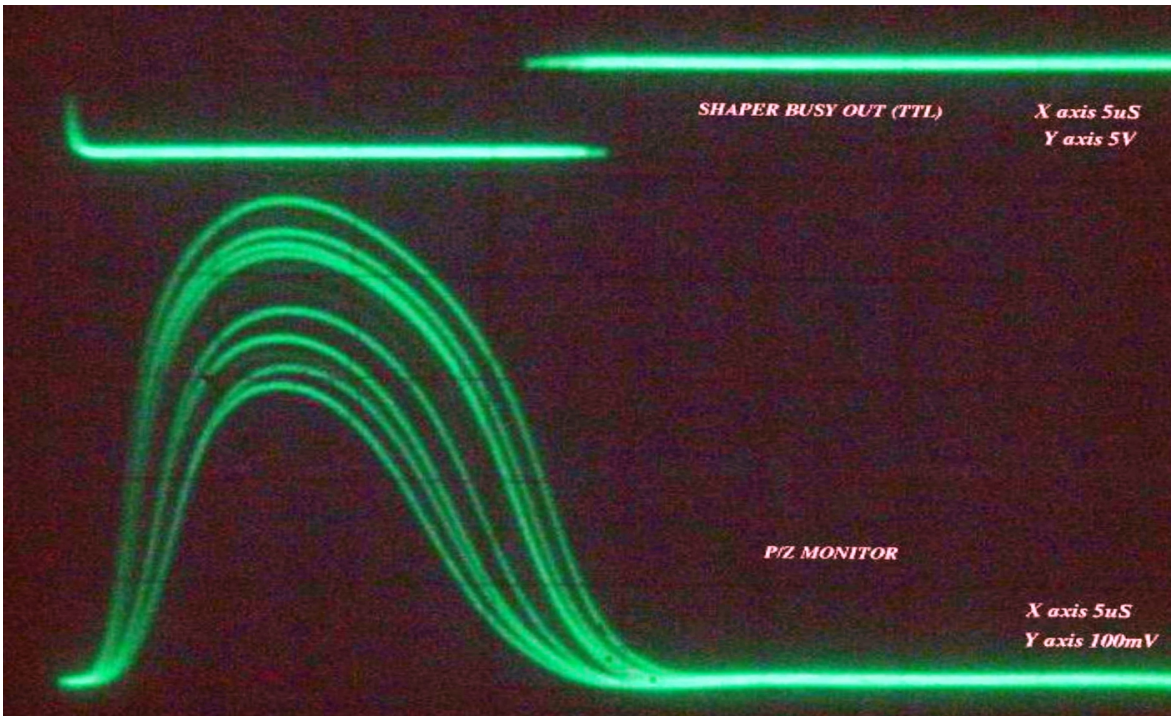
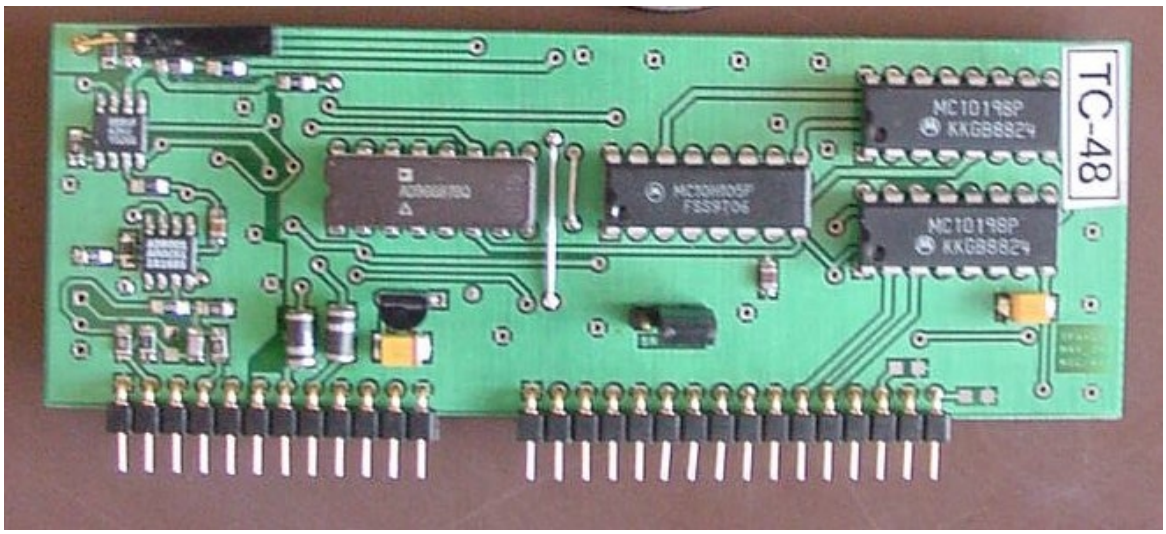
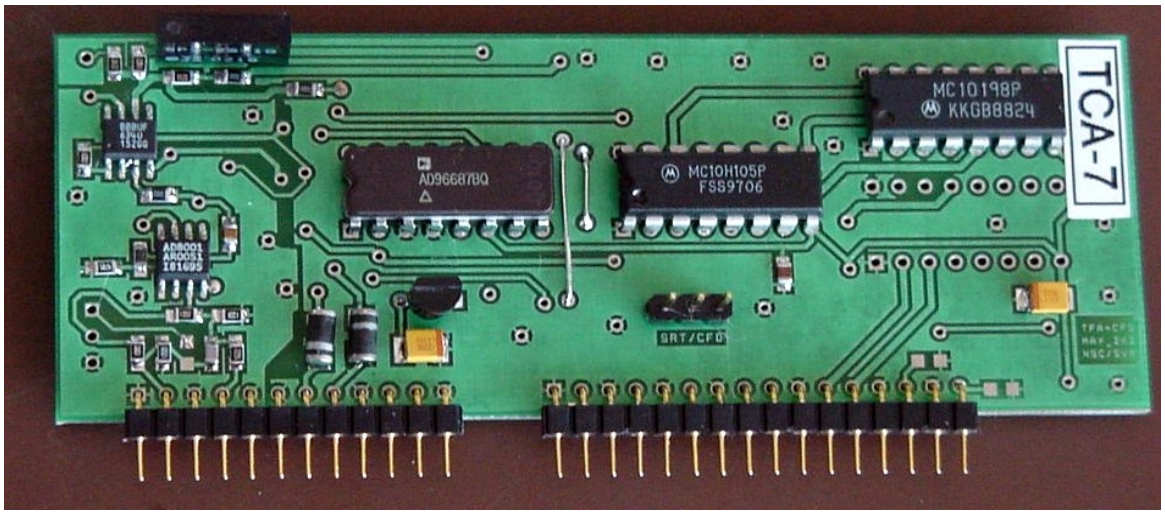


Fig: TFA+CFD card for Germanium an optional ACS detectors





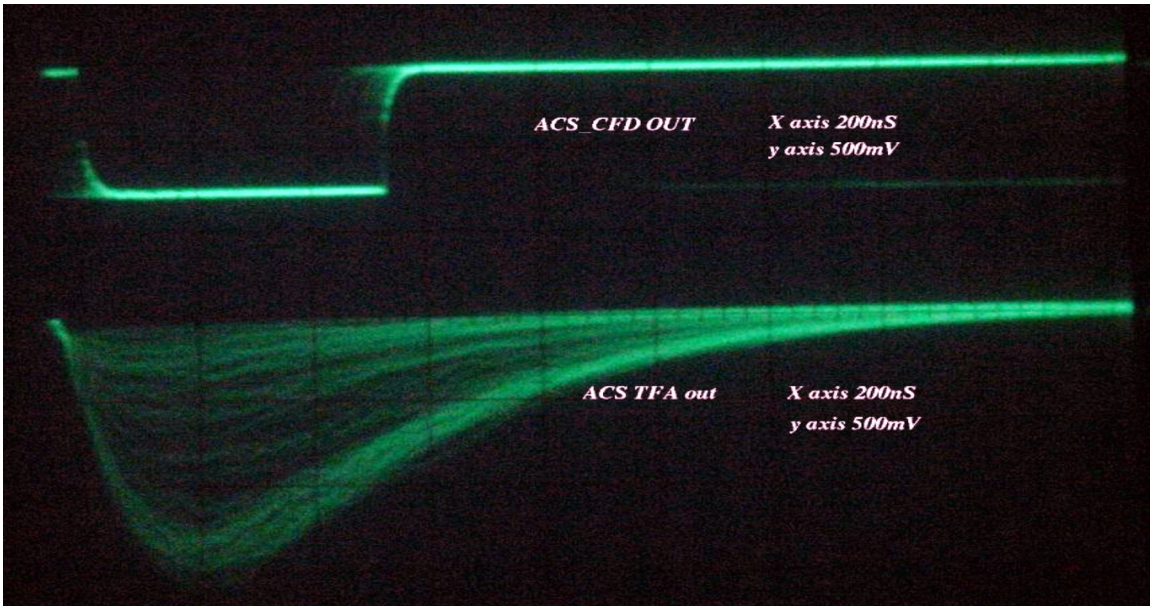
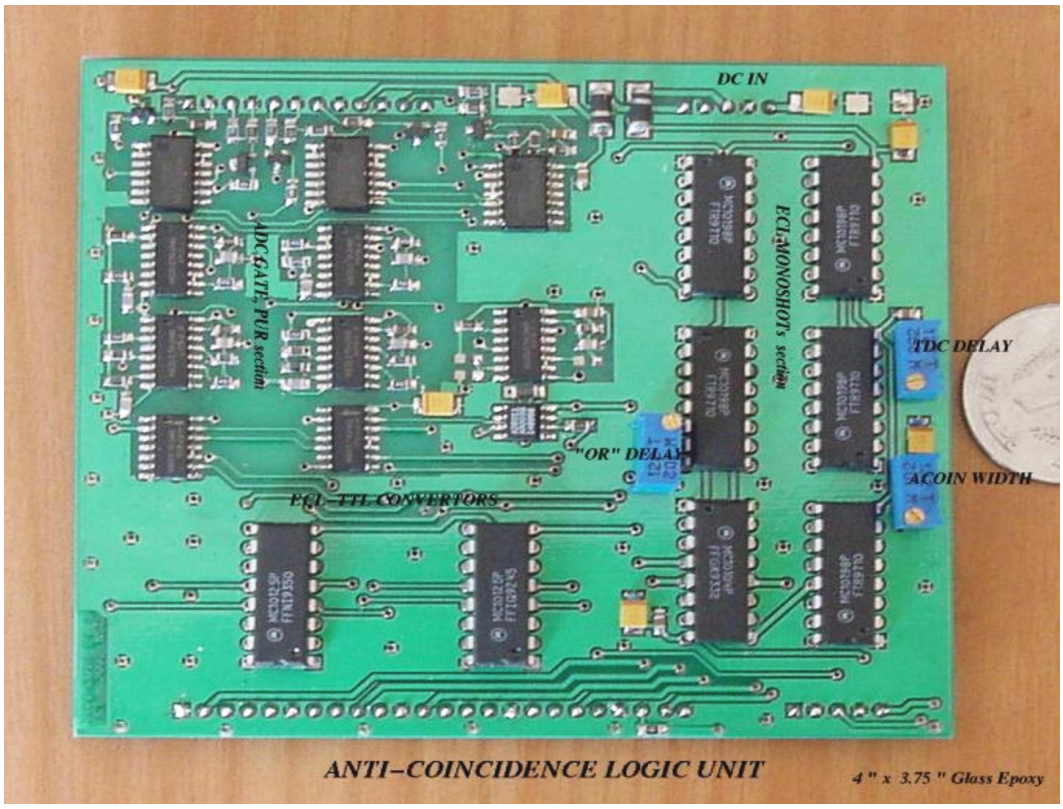
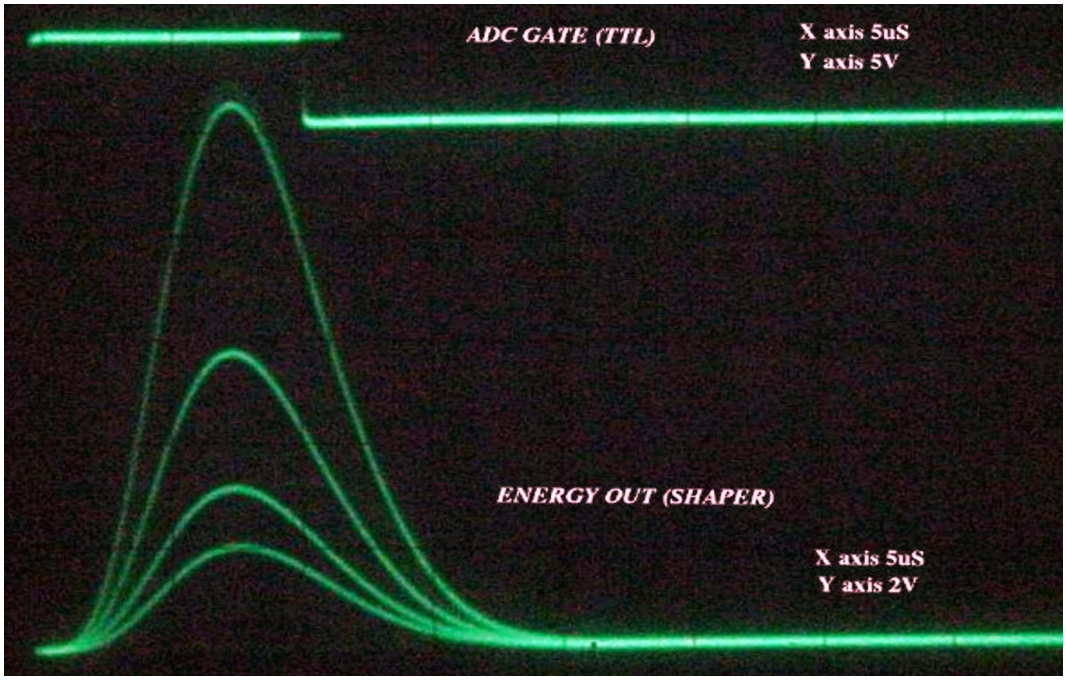


Fig: ACLogic card with typical signals monitored





Testing of LEPS at VECC, Kolkatta with modified cards in IUAC Clover modules :

2. One Shaper card and one Timing card of the existing Clover module is replaced by the modified & corrected Shaper and Timing card.

3. The gain of Clover module is set to gain maximum, i.e., 500 keV full scale, no jumper. Similarly with one jumper and two jumpers, the gains were set.

	Calibration	Pulse height for 30 keV X-ray of ^{133}Ba
No jumper	: 0.06 keV/ch	280 mV
One jumpers	: 0.11 keV/ch	140 mV
Two jumpers	: 0.16 keV/ch	100 mV

So the **gain factor seems to be o.k. with different jumper selection**.

4. Similar gain as set in Clover module was set in this 2024 amplifier.
356 keV peak of ^{133}Ba was kept at the same channel, though some nonlinearity was found towards the lower energy.

It is observed that the **resolution is worse with Clover module** in lower gain. But it has improved compared to previous LEPS card made.

	Resolution at 356 keV
Canberra 2024 spectroscopy amplifier	1.43 keV 1.41 keV 1.48 keV
Clover module with modified card	1.44 keV (500keV gain) 1.58 keV (1MeV gain) 1.98 keV (2MeV gain)

5. The new Card also shows some noise from time to time (A spike comes in spectra at lowest channel sometime).

6. The data was taken in coincidence mode. When the threshold of the card is working properly,

For full scale gain = 500 keV,

Source	cut upto	Pulse Height	Threshold
^{133}Ba	Noise		+13.9 mV
	30 keV x-ray	280 mV	-281 mV
	81 keV	140 mV	-1.135 mV

Thanks to Mrs.Sharmista Mukherjee & her Colleagues @ VECC.

	Mother Board	1	per Module	
Sl.No	Item Descriptions	Qty/PCB	Source	Source/Code No.
1	PCB, FR-4, 1.6MM, 70uM,	1	Ancomp /Loca	Dry image process, Silk
	Model 2k6			Solder mask done with
	50PPM, 0805, MFR, 1% Resistor		IMPORT	
2	22	2	MERITEK	RN73-G-2A-TE-XXX-F
3	33.2	1	MERITEK	RN73-G-2A-TE-XXX-F
4	100	5	MERITEK	RN73-G-2A-TE-XXX-F
5	220	11	MERITEK	RN73-G-2A-TE-XXX-F
6	332	1	MERITEK	RN73-G-2A-TE-XXX-F
7	750	1	MERITEK	RN73-G-2A-TE-XXX-F
8	10k	5	MERITEK	RN73-G-2A-TE-XXX-F
9	220K	4	MERITEK	RN73-G-2A-TE-XXX-F
10	1K	1	MERITEK	RN73-G-2A-TE-XXX-F
11	1.2K	4	MERITEK	RN73-G-2A-TE-XXX-F
12	2K	4	MERITEK	RN73-G-2A-TE-XXX-F
13	0 OHMS	2	MERITEK	RN73-G-2A-TE-XXX-F
14	1.5K*	4	MERITEK	RN73-F-2A-TE-XXX-F
15	1K *	2	MERITEK	RN73-F-2A-TE-XXX-F
14	LED (1210)	1	Local	
15	TORROID T-12	5	Local	
16	SIP-5-255, Delayline	4	IMPORT	RHOMBUS
17	P9105-32-11-1 strip	4	Local	Protectron Electromech.
	0.1” pitch DOUBLE ROW, SMD HEADER)			
18	0.1” double row Headers strip	1	Local	Protectron Electromech.
19	0.1” Header Jumpers	10	Local	Protectron Electromech.
20	Cfu pins 4 pins set for LED	2	Local	
21	BD680A POWER TRANSISTOR	1	Local	SGS THOMSON
22	Heatsink kit for above	1	Local	
23	3mm LED RED	4	Local	
24	2N3904A Plastic thru hole	1	Local	PHILIPS/DIODE INC.
25	2N3906A Plastic thru hole	1	Local	PHILIPS/DIODE INC.
26	2N3906A SOT-23	1	Local	PHILIPS/DIODE INC.
27	BAT54S SOT-23	4	Local	PHILIPS/DIODE INC.
28	1N4003 SMD MINIMELF 1A Diode	1	Local	PHILIPS/DIODE INC.
29	ADR03BR SOIC	1	IMPORT	ANALOG DEVICES
30	LT1361CS8	1	IMPORT	LINEAR TECHNOLOGY
31	SN74AHCT123A SOIC-16	2	IMPORT	TEXAS INST
32	Potentiometer trimpot	18	IMPORT	SPECTROL/VISHAY
	M43P-103-K-B40-T602			
	10k, Panel type			
33	2MM Test point BS-3/RED..	6	Local	ELMECH INDIA
34	LED Holder 3mm Plastic	4	Local	
35	PTFE Hookup #26swg/x7	1M	Local	
36	0552-2-15-15-11-14-10-0	270	IMPORT	Mill-max

Table 1: List of Components required:

	Multilayer Ceramic chip capacitors			
37	0805-5-C-104-K-A-T-2-A	82	IMPORT	AVX
38	0805-5-C-103-K-A-T-2-A	~25	IMPORT	AVX
39	1nF/0805/50V/X7R	1	Local	
	TANTALUM CAPACITORS			
40	TAJC106K035R	13	IMPORT	AVX
41	TAJB106K035R	12	IMPORT	AVX

Cabinet and related Hardwares

Sl.No	Item Descriptions	Qty/PCB	Source	Source/Code No.
1	ERA.00.250.CTL	44x	IMPORT	LEMO CONNECTOR NIM
2	GCD.00.020.LA	44x	IMPORT	Earth cap
3	GRA.00.269.GG (grey)	8X	IMPORT	GREY WASHER
4	DCG.91.149.OTN	1X	IMPORT	WRENCH
5	M17-093-RG178	100feet	IMPORT	Belden Cables-WHITE
6	CABINET_000102-00	1X	IMPORT	Mech-Tronics
7	CONNECTORS NIM_100-10	1X	IMPORT	Mech-Tronics
8	3CORE Flat plastic/PTFE.wire	20feet	Local	
9	Panel preparation Drawing attached	1X	Local	***On requirement***
10	PanelScrren printing attached	1X	Local	***On requirement***

	Shaping Amplifier card	4 card per Module		
Sl.No	Item Descriptions	Qty/PCB	Source	Source/Code No.
1	PCB, FR-4, 1.6MM, 70uM,	1X	Ancomp /Loca	Dry image process, Silk
	Model 2k6NSC-JULY 2K2			Solder mask done with
	SHAPER_PT5_CORR			
	25PPM, 0805, MFR, 1% Resistor			**MERITEK**
2	22	1X	IMPORT	RN73-F-2A-TE-XXX-F
3	6.8K	3X	IMPORT	RN73-F-2A-TE-XXX-F
4	680	1X	IMPORT	RN73-F-2A-TE-XXX-F
5	1.5K	4x	IMPORT	RN73-F-2A-TE-XXX-F
6	1.3K	1X	IMPORT	RN73-F-2A-TE-XXX-F
7	2K	1X	IMPORT	RN73-F-2A-TE-XXX-F
8	330	1X	IMPORT	RN73-F-2A-TE-XXX-F
9	100	1X	IMPORT	RN73-F-2A-TE-XXX-F
10	3.32K	1X	IMPORT	RN73-F-2A-TE-XXX-F
11	10K	1X	IMPORT	RN73-F-2A-TE-XXX-F
12	5.1K	1X	IMPORT	RN73-F-2A-TE-XXX-F
	50PPM, 0805, MFR, 1% Resistor			
13	22	8X	IMPORT	RN73-G-2A-TE-XXX-F
14	47.5	3X	IMPORT	RN73-G-2A-TE-XXX-F
15	100	3X	IMPORT	RN73-G-2A-TE-XXX-F
16	1K	12X	IMPORT	RN73-G-2A-TE-XXX-F
17	2K	1X	IMPORT	RN73-G-2A-TE-XXX-F
18	22K	1X	IMPORT	RN73-G-2A-TE-XXX-F
19	10K	5X	IMPORT	RN73-G-2A-TE-XXX-F
20	15K	2X	IMPORT	RN73-G-2A-TE-XXX-F
21	511	2X	IMPORT	RN73-G-2A-TE-XXX-F

22	47.5K	5x	IMPORT	RN73-G-2A-TE-XXX-F
23	1.5K	1X	IMPORT	RN73-G-2A-TE-XXX-F
24	100K	1X	IMPORT	RN73-G-2A-TE-XXX-F
25	5.6K	1x	IMPORT	RN73-G-2A-TE-XXX-F
26	3.32K	2X	IMPORT	RN73-G-2A-TE-XXX-F
27	10	1X	IMPORT	RN73-G-2A-TE-XXX-F
	Multilayer Ceramic chip capacitors			
28	0805-5-C-104-K-A-T-2-A	30X	Local	AVX
29	1206-5-C-224-K-A-T-2-A	1X	Local	AVX
30	0805-5-C-223-K-A-T-2-A	2X	Local	AVX
	TANTALUM CAPACITORS			
31	TAJC106K035R	2X	IMPORT	AVX
32	TAJB106K035R	14X	IMPORT	AVX
33	TAJA155K025R	2X	IMPORT	AVX
	COG/NPO Multilayer capacitors			
34	1206, 50V, 1500PF	3X	IMPORT	AVX
35	0805, 50V, 1000PF	6X	IMPORT	AVX
36	0805, 50V, 22PF	2X	IMPORT	AVX
37	0805, 50V, 220PF	2X	IMPORT	AVX
38	0805, 50V, 330PF	2X	IMPORT	AVX
	SOIC-8 SMD PACKAGES			
39	LT1361CS8	2X	IMPORT	LINEAR TECHNOLOGY
40	AD829AR	2X	IMPORT	ANALOG DEVICES
41	AD835 AR	1X	IMPORT	ANALOG DEVICES
42	BUF634U	1X	IMPORT	Burr-Brown/TI
43	CA3080S	1X	IMPORT	HARRIS
44	MAX912CSE	1X	IMPORT	MAXIM
45	LM555CM	1X	IMPORT	National Semi.
46	MM74HC02M	1X	IMPORT	National Semi.
47	AD823AR	1X	IMPORT	ANALOG DEVICES
	SMD PACKAGES			
48	1N4003 SMD MINIMELF 1A Diode	2X	IMPORT	PHILIPS/DIODE INC.
49	BAV99/SOT-23	4x	IMPORT	PHILIPS/DIODE INC.
50	BAT54 SOT-23	2X	IMPORT	PHILIPS/DIODE INC.
51	BZX84C4V7 SOT-23	1X	IMPORT	PHILIPS/DIODE INC.
52	BZX84C8V2 SOT-23	1X	IMPORT	PHILIPS/DIODE INC.
53	BAT54A SOT-23	1X	IMPORT	PHILIPS/DIODE INC.
54	BAT54S SOT-23	1X	IMPORT	PHILIPS/DIODE INC.
55	MMBF4416L/SOT-23	1X	IMPORT	PHILIPS/DIODE INC.
56	PMBT3906/SOT-23	2X	IMPORT	PHILIPS/DIODE INC.
57	PMBT3904/SOT-23	1X	IMPORT	PHILIPS/DIODE INC.
	CONNECTORS			**Single row 32pins 10uM gold**
Interconnects, Single Row,Rightangle Pin header				**0.1"Grid 0.018" LEAD Dia.**
58	*399-10-132-010-009*	1x	IMPORT	Mill-max

	TFA + CFD CARD	5 cards per Module		
Sl.No	Item Descriptions	Qty/PCB	Source	Source/Code No.
1	PCB, FR-4, 1.6MM, 70uM,	1 x	Ancomp /Loca	Dry image process, Silk
	Model MAY2K2			Solder mask done with
	TFA+CFD			
	50PPM, 0805, MFR, 1% Resistor			***XXX: FILL-IN***
2	22	3X	IMPORT	RN73-G-2A-TE-XXX-F
3	220	3X	IMPORT	RN73-G-2A-TE-XXX-F
4	332	2X	IMPORT	RN73-G-2A-TE-XXX-F
5	0	2X	IMPORT	RN73-G-2A-TE-XXX-F
6	1K	2X	IMPORT	RN73-G-2A-TE-XXX-F
7	10	1X	IMPORT	RN73-G-2A-TE-XXX-F
8	51	1X	IMPORT	RN73-G-2A-TE-XXX-F
9	22K	3X	IMPORT	RN73-G-2A-TE-XXX-F
10	4.75K	2X	IMPORT	RN73-G-2A-TE-XXX-F
11	47.5K	1X	IMPORT	RN73-G-2A-TE-XXX-F
12	1.2K	1X	IMPORT	RN73-G-2A-TE-XXX-F
13	750	1X	IMPORT	RN73-G-2A-TE-XXX-F
14	2K	7x	IMPORT	RN73-G-2A-TE-XXX-F
15	47.5	4x	IMPORT	RN73-G-2A-TE-XXX-F
16	3.32K	2X	IMPORT	RN73-G-2A-TE-XXX-F
17	511	11X	IMPORT	RN73-G-2A-TE-XXX-F
18	100	5X	IMPORT	RN73-G-2A-TE-XXX-F
19	110	5X	IMPORT	RN73-G-2A-TE-XXX-F
20	82 OHM, MFR, 1% THROUGH HOLE	1X	Local	
	Multilayer Ceramic chip capacitors			
21	0805-5-C-104-K-A-T-2-A	13X	Local	AVX
22	0805-5-C-103-K-A-T-2-A	2X	Local	AVX
	INDUCTORS SMD 1210			
23	47uH	3X	IMPORT	AVX
	TANTALUM CAPACITORS			
24	TAJB106K035R	10X	IMPORT	AVX
	COG/NPO Multilayer capacitors			
25	0805, 50V, 470PF	2X	IMPORT	AVX
26	0805, 50V, 4.7PF	1X	IMPORT	AVX
27	0805, 50V, 220PF	2X	IMPORT	AVX
28	0805, 50V, 10PF	1X	IMPORT	AVX
	SOIC-8 SMD PACKAGES			
29	AD96687BQ	1X	IMPORT	LINEAR TECHNOLOGY
30	AD8011AR	1X	IMPORT	ANALOG DEVICES
31	MC10198P	2X	IMPORT	ANALOG DEVICES
32	BUF634U	1X	IMPORT	Burr-Brown/TI
33	MC10H105P	1X	IMPORT	HARRIS
34	SP3-25-10	21X	IMPORT	RHOMBUS, 25nS, 100Zo

	SMD PACKAGES			
35	1N4003 SMD MINIMELF 1A Diode	2X	IMPORT	PHILIPS/DIODE INC.
36	BAV70/SOT-23	3X	IMPORT	PHILIPS/DIODE INC.
37	BAT54C /SOT-23	1X	IMPORT	PHILIPS/DIODE INC.
38	BRF92A/ SOT-23	2X	IMPORT	PHILIPS/DIODE INC.
	CONNECTORS			**Single row 32pins 10uM gold**
Interconnects, Single Row,Rightangle Pin header				**0.1"Grid 0.018" LEAD Dia.**
39	*399-10-132-010-009*	1x	IMPORT	Mill-max
40	RIGHT ANGLE 0.1" Header , SINGLE ROW X3	1X	Local	Protectron Electromech.

NTICOINCIDENCE LOGIC CARD

1 PER INGA MODULE

Sl.No	**Item Descriptions**	**Qty/PCB**	**Source**	**Source/Code No.**
1	PCB, FR-4, 1.6MM, 70uM,	1X	Ancomp	Dry image process, Silk
	Model PT-4, 2003		/Local	Screen, Solder Mask
	ACLOGIC CARD			
	50PPM, 0805, MFR, 1% Resistor			***XXX: FILL-IN***
2	220	10X	IMPORT	RN73-G-2A-TE-XXX-F
3	4.7	1x	IMPORT	RN73-G-2A-TE-XXX-F
4	10	6X	IMPORT	RN73-G-2A-TE-XXX-F
5	1.3K	1X	IMPORT	RN73-G-2A-TE-XXX-F
6	475	8X	IMPORT	RN73-G-2A-TE-XXX-F
7	22K	4x	IMPORT	RN73-G-2A-TE-XXX-F
8	2K	3X	IMPORT	RN73-G-2A-TE-XXX-F
9	1.2K	1X	IMPORT	RN73-G-2A-TE-XXX-F
10	10K	4x	IMPORT	RN73-G-2A-TE-XXX-F
11	1.5K	5X	IMPORT	RN73-G-2A-TE-XXX-F
12	47.5	10X	IMPORT	RN73-G-2A-TE-XXX-F
13	3.32K	13X	IMPORT	RN73-G-2A-TE-XXX-F
14	511	8X	IMPORT	RN73-G-2A-TE-XXX-F
15	1.6K	1X	IMPORT	RN73-G-2A-TE-XXX-F
16	110	30X	IMPORT	RN73-G-2A-TE-XXX-F
17	1K	1x	IMPORT	RN73-G-2A-TE-XXX-F
	Multilayer Ceramic chip capacitors			
17	0805-5-C-104-K-A-T-2-A	10X	Local	AVX
18	0805-5-C-103-K-A-T-2-A	30X	Local	AVX
	POTENTIOMETER			
19	M64W-202-K-B40	3X	IMPORT	VISHAY
	TANTALUM CAPACITORS			
20	TAJB106K035R	4x	IMPORT	AVX
21	TAJB225K035R	5X	IMPORT	AVX
22	TAJC106K035R	3X	IMPORT	AVX

List of Cables & Wires required for Interconnection inside Module

Standard lengths to be cut as per this table.						
NAME	***LENGTH***	***NAME***	***LENGTH***			
	Inches		***Inches***			
FRONT PANEL CONNECTIONS						
A_COIN	6.5	BUSY_A	5			
OR_P	6	BUSY_B	5			
TDC	6.5	BUSY_C	5			
MASTER_GATE (M_GATE)	6	BUSY_D	5			
GATE_A	5	P/Z_MON_A	5.5			
GATE_B	5	P/Z_MON_B	5.5			
GATE_C	6	P/Z_MON_C	5.5			
GATE_D	6	P/Z_MON_D	5.5			
EOUT_A	11					
EOUT_B	10	WALK_MON_A	9			
EOUT_C	10	WALK_MON_B	10			
EOUT_D	9	WALK_MON_C	10			
		WALK_MON_D	11			
ACS TFA (TFA_M)	12	WALK_MON-ACS	10			
REAR PANEL CONNECTIONS						
EIN_A	4	ACS_CFD	9			
EIN_B	4	A_CFD	10			
EIN_C	4	B_CFD	9			
EIN_D	4	C_CFD	8			
TIME_IN A	3 & 3.25	D_CFD	6.5			
TIME_IN B	3 &3					
TIME_IN C	3&2	PUR	8			
TIME_IN D	3 & 2	PUR:Short 4 Lemos inner contacts and use				
TIME_IN ACS	6	Lug for ground connection.				

CORE Splitted PTFE WIRES						
BLR_A	4.5	LLTH_A	3.5	Use Low noise wire/GLN-196A/U		
BLR_B	4.5	LLTH_B	3.5	LLTH_A	8	
BLR_C	4.5	LLTH_C	4	LLTH_B	9	
BLR_D	4.5	LLTH_D	4	LLTH_C	10	
		LLTH_ACS	4	LLTH_D	11	
				LLTH_ACS	10	
P/Z ADJ. A	4.5	WALK_ADJ. A	3.5	Temp	10	
P/Z ADJ. B	4.5	WALK_ADJ. B	3.5			
P/Z ADJ. C	4.5	WALK_ADJ. C	3.5			
P/Z ADJ. D	4.5	WALK_ADJ. D	4			
		WALK_ADJ. ACS	4			

Connections for Potentiometers are done through 3core Flat splitted PTFE wires, SWG26, multistrand.

Instructions

Cable : RG178B/U, Make: BELDEN or equ.
Use cautiously-sharp Industrial knife/sleeve remover to remove sleeve
Use scissors/cutter to remove braid.
Use brush to clean braid bits which may cause short circuit.
Start the connection from connector ends with earth caps in case of Coaxial cable.
Start the connections form PCB incase of teflon/plastic wire.

Remove only 2mm-3mm-5mm lenth for coax & low noise cables (inner-dielectric-braid)ie. 10mm.
Remove 10mm towards pot end and 6mm towrds PCB end of PTFE wires

The lengths given are always bit longer than required. Trim the length for neat assembly
And secure them heat shrink tubes and or 10mm Cable ties where ever applicable.

Internet Web resources :

http://www.mech-tronics.com/
http://www.vishay.com/
http://www.avx.com/
http://www.lemosa.com/
http://www.rhombus-ind.com/
Http://www.analogdevices.com/
Http://www.linear.com/
Http://www.protectron-electromech.com/
http://www.mill-max.com/
http://www.meritekusa.com/
http://www.smd-in.com/