TECHNICAL REPORT

TITLE	: Technical Report on TIME TO ANALOGUE CONVERTER for Neutron Array at IUAC.
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CATEGORY	: Instrumentation
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for Neutron Array at IUAC

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Abstract: **At IUAC, we have succesfully developed and implemented a general purpose and compact TIME TO AMPLITUDE (TAC) converter for the ongoing Large Neutron Array[1] at IUAC. The TAC daughter card contains a TAC Hybrid Microchip BMC1522 alongwith level converters, power supply circuits and gain cum buffer circuit. Though recommanded for 500nS range, we have adopted the same for 100nS range and characterised its performances in this report.**

Acknowledgment:

We would like to thank Dr. Swapan Kumar Dutta of Neutron Array at IUAC for specifying and evaluating overall timing functioning of the prototype and preproduction versions of the module. Our sincere thanks to Dr.Amit Roy, and Ajith Kumar. B.P, for their constant encouragement and providing the necessary infrastructure in order to complete this project successfully.

Specifications:

Time to Amplitude Converter

TAC Range	:100nS (Capacitor : 27pF / SM type)	
Resolution	: better than 50pS [2]	
Drift/Thermal stability	: Short term (0-15 min)	: 85 pS
	Long term (15-200 min)	: 40pS
Inputs	:START/RESET, STOP of Fast NIM type.	
Output range & Width	: 0 – 10Volts, 2.5μS	
DC Supply required	:±12Volts and -6V (750 mWatts)	
Card Dimension	:44mm, x 70mm x 10mm	

Note:

Refer the Data sheet for different TAC range.

Different Type Capacitors may be tried for best thermal stability or Drift Characteristics.

Introduction:

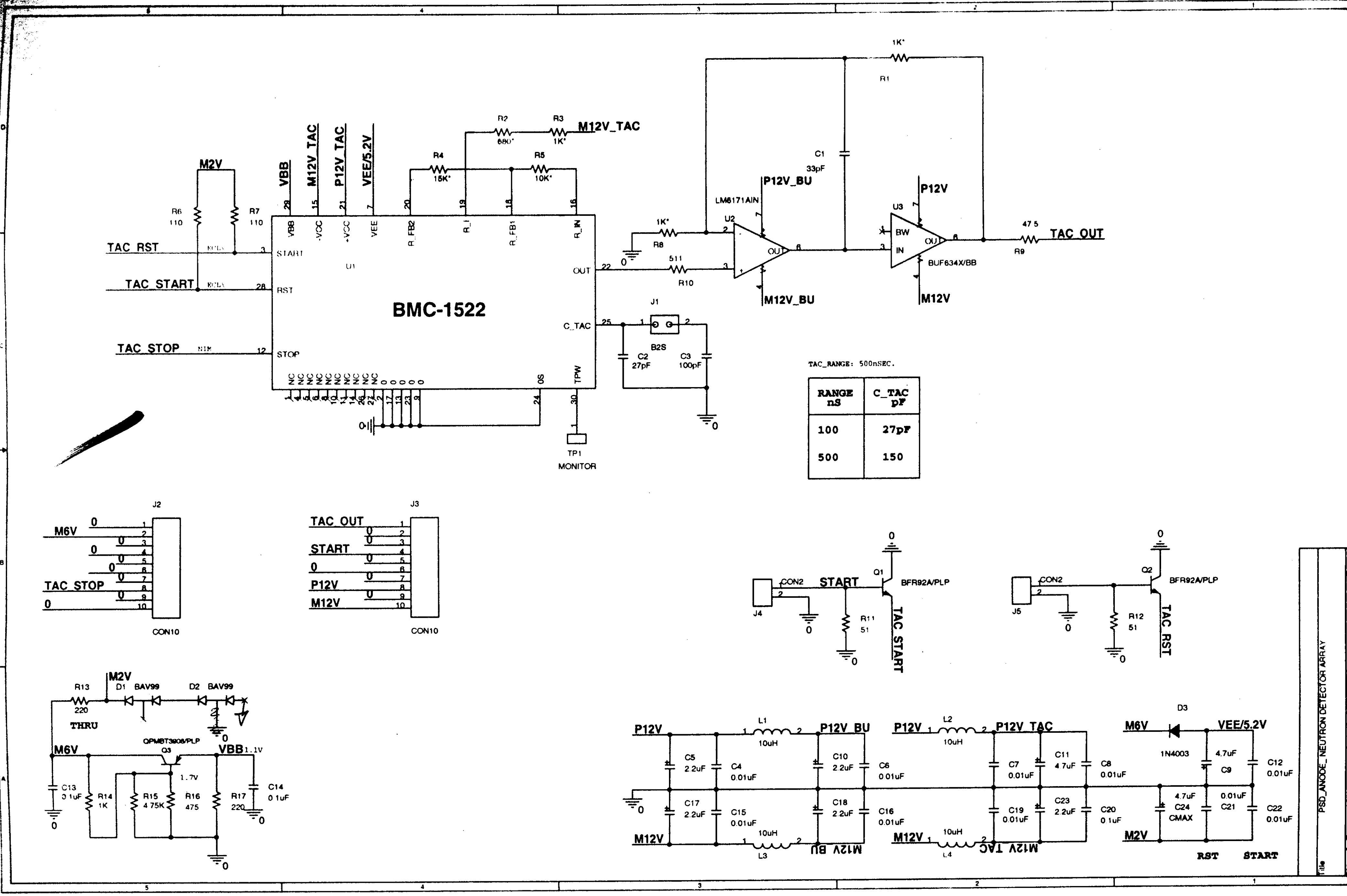
Time to Amplitude (TAC) is a very essential circuit function utilised for various Nuclear experiments in a accelerator laboratory. The commercial Single/Multiple width TAC modules available are of general purpose in nature. They are also costly, bulky and require additional level converters, cables and connectors in a experimental setup.

In order to cater similar applications, we have successfully developed a compact TAC daughter card, which can be incorporated into any custom Nuclear Electronic modules. They are self contained, having required non standard power supplies, level converters, amplifier cum buffer to drive a low impedance coaxial cable.

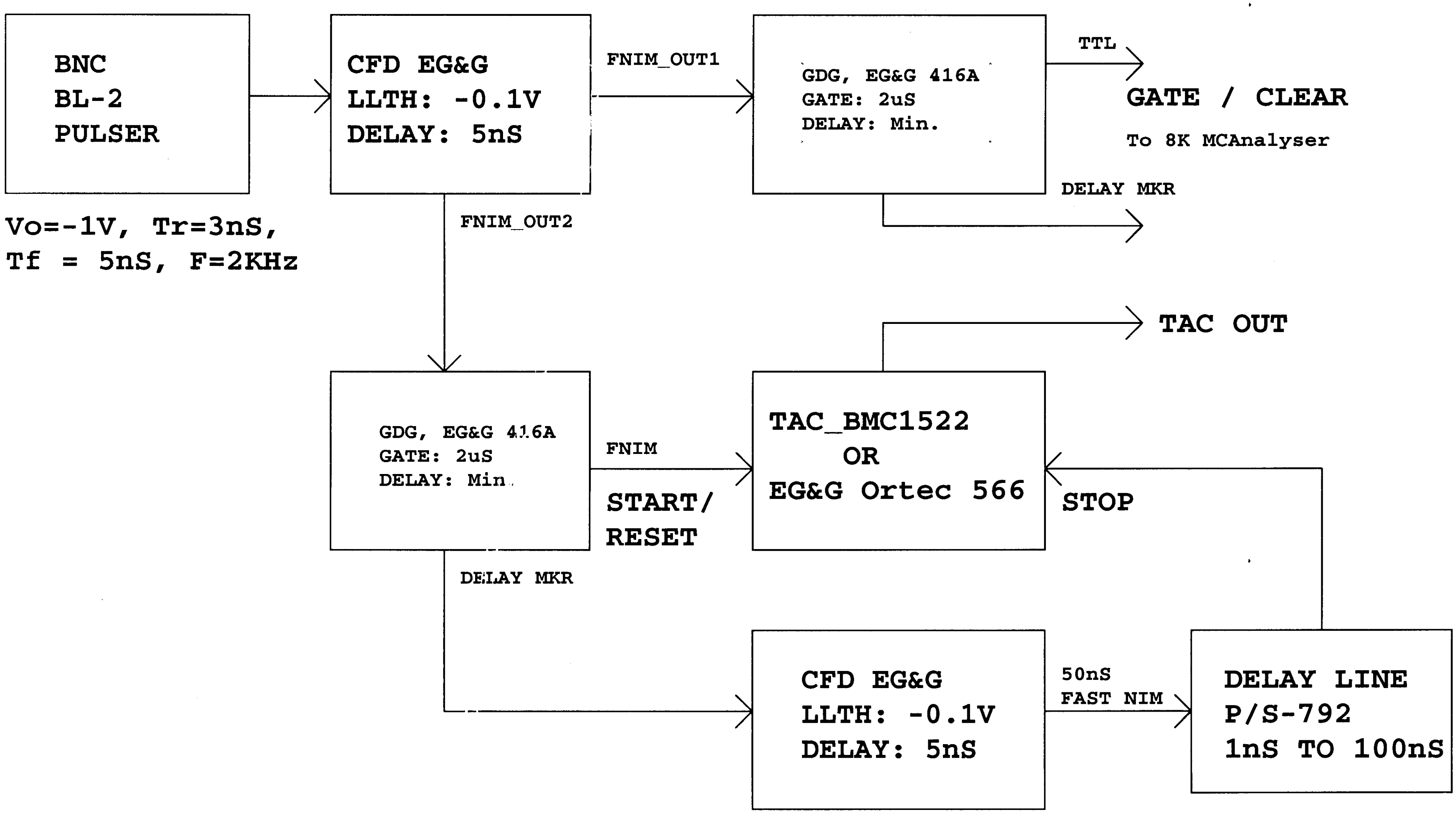
Principle of Operations:

The detail working principle of TAC Hybrid Micro Chip BMC-1522, developed by BARC and produced by M/s.BEL and detail circuit implementation are made available within this report. Apart from the HMC, circuit board contains a non-standard biasing supply (VBB- 1.1V) required by this chip, derived from M6V supply line. The required level converters (FNIM – ECL) are also implemented with a single transistor. The TAC range can be determined by Capacitor selection or Charging current (alter R2, R3) programming. The charging current is fixed and only Capacitor is changed to alter the TAC range. For example: 27pF is chosen for ~100 nS range in this design. High quality resistors (MFR, 1%, 25PPM) and Capacitor (Silver Mica) are used for best performance. The supply lines are filtered with LC type filters.

The TAC HMC is capable of 0-5V for the programmed TAC range. In order to make it identical to a commercial module, the output is amplified and buffered through composite amplifier containing LM6171 (WB Opamp) and BUF634 Buffer to obtain the dynamic output range 0- 10 Volts.



RANGE nS	C_TAC pF
100	27pF
500	150



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Title	TEST SET UP OF TAC Modules	
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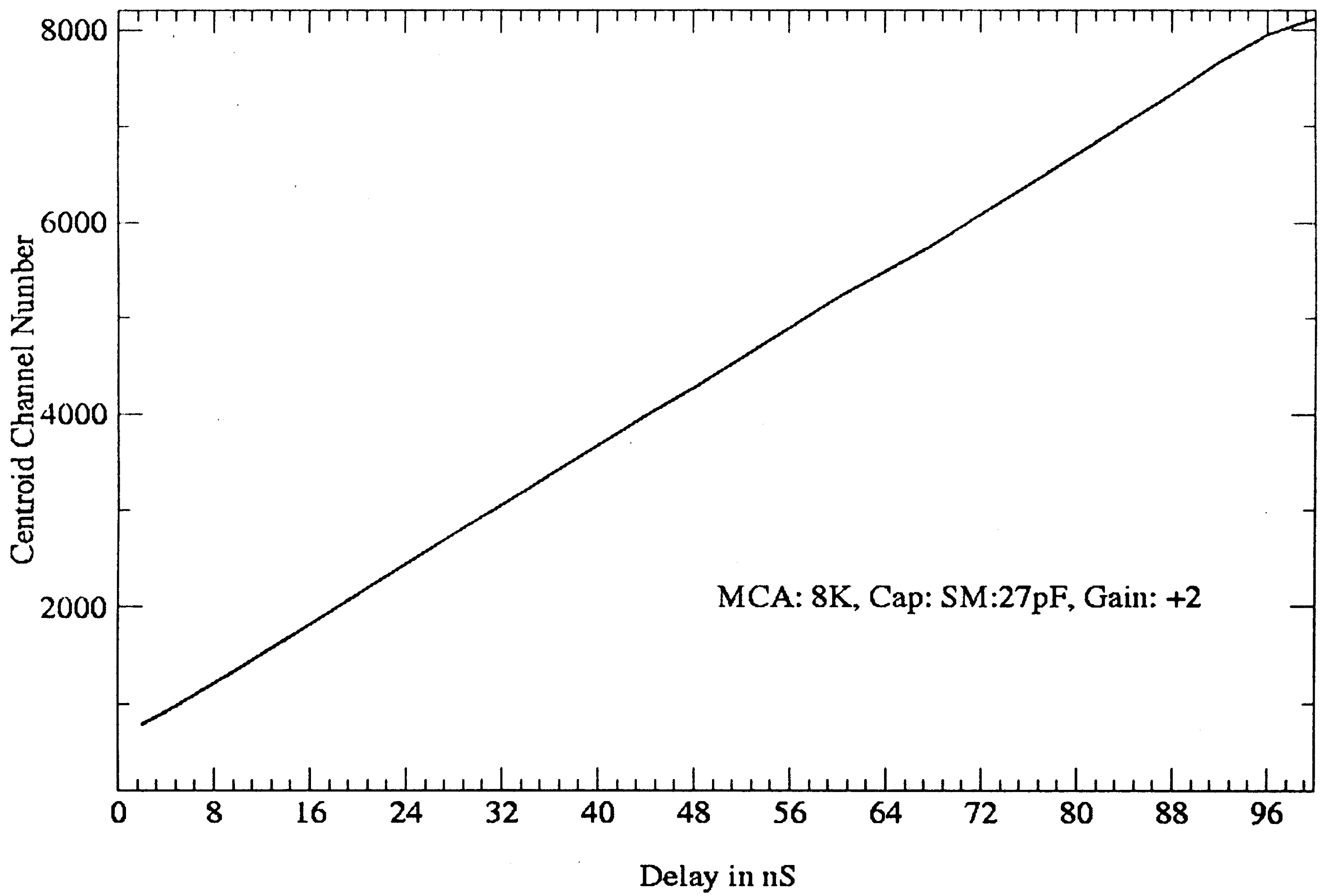
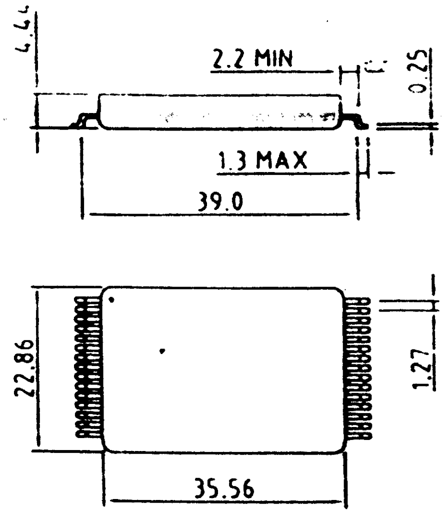
Date: Monday, April 24, 2006	Sheet 1 of 1	

Performance test for BMC1522_TAC-100nS

Delay vs centroid



HYBRID MICROCIRCUIT
BMC 1522
TIME TO AMPLITUDE CONVERTER



Note: Dot indicates pin no. 1

GENERAL : BMC 1522 is a time to amplitude converter. The TAC gives analog voltages propotional to Time between start and stop pulse. As shown in Block Diagram. A capacitor is discharged by constant current source initiated by start pulse On arrival of NIM STOP pulse within the full scale, it stops discharging ramp. The difference between the initial and final voltage is propotional to the time between start and stop pulse. It can be used as time to amplitude converter. It is housed in a 30 pin hermetically sealed flat package. It comes as surface mount devices.

Absolute Maximum Ratings:

Operating temperature : 0°C to 70°C

Storage temperature : -25°C to 85°C

* For safe and proper functioning of the device these rating should not exceed.

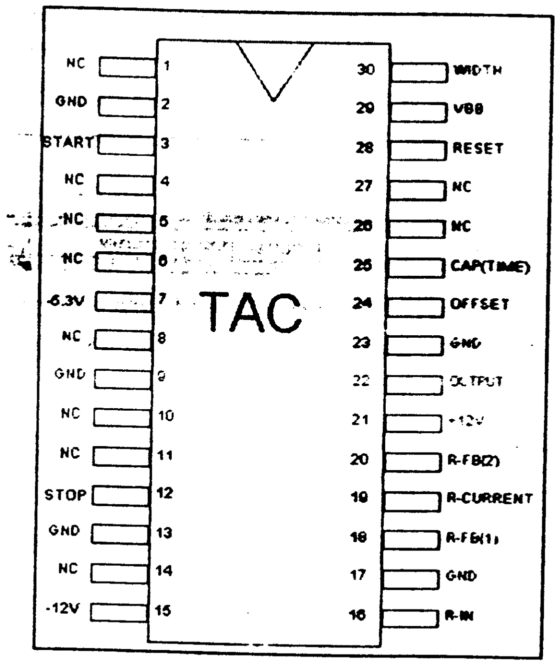
ELECTRICAL CHARACTERISTICS (T_A=25°C, +Vcc=+12V, -Vcc=-12V, VEE=-5.3V, VBB=-1.1V)

Sl. No.	Parameters	Limits			Unit	Test Condition
		Min.	Typ.	Max.		
1.	Output					
	Full Scale Voltage	0	- - -	5	V	Start : ECL
2.	Range min-max	- - -	- - -	500n	S	Stop : FAST NIM
3.	Resolution (with full scale of 500ns)	- - -	- - -	250p	S	RESET : ECL/TTL
4.	Power consumption	--	- - -	500	mW	

Revd.	Issue: 01	DOC CODE:DS	DRG. NO: 2522-1	SH:1/2
Apvd.	Date:01.03.04	HELD IN:HMC	DATA SHEET	

TAC (TIME TO AMPLITUDE CONVERTOR) HYBRID

INTRODUCTION: Time between START and STOP is converted into equivalent analog Voltage. During the interval of Start & Stop trigger a Capacitor is discharge by constant current source initiated by START pulse. The TAC is initialized by common reset.



PIN DIAGRAM

KEY SPECIFICATION:

Start	: ECL
Stop	: Fast NIM
Reset	: TTL
Output Full scale voltage	: 0 to +5V
Range: min -max	: 500ns to 100us by ext. resistor
Power Supplies:	: ±12v,-5.3v
Power consumption:	: less than 1Watt.
Package	: 30 PIN
Reference voltage (current)	: inbuilt

POWER SUPPLY :

+12V 20mA, -12V 25mA, -5v 45mA,

Power dissipation : appox. 750mW

Temperature : 0 to +70 °C

APPLICATION:

Time of flight spectroscopy

Laser induced chemical studies.

[redacted]

PIN DESIGNATION [redacted]

PIN	FUNCTION	DESCRIPTION	PIN	FUNCTION	DESCRIPTION
1	NC	No Connection	[redacted]	[redacted]	[redacted] for gain adjustment
2	GND	Analog Ground	17	GND	Analog Ground
3	START	ECL input	18	R-FB(1)	Gain adg.Resistor input side of op-amp
4	NC	No Connection	19	R-CURRENT	Full scale adj.Resistor
5	NC	No Connection	20	R-FB(2)	Gain-adj Resistor op-amp output point
6	NC	No Connection	21	+12V	Positive power supply
7	-5.3V	Negative power supply	22	OUTPUT	Final Output of TAC
8	NC	No Connection	23	GND	Analog Ground
9	GND	Analog Ground	24	OFFSET	Offset adjstment
10	NC	No Connection	25	CAP(TIME)	Timing Capacitor
11	NC	No Connection	26	NC	No Connection
12	STOP	NIM input	27	NC	No Connection
13	GND	Analog Ground	28	RESET	Reset the output
14	NC	No Connection	29	VBB	Negative 1.1v internal
15	-12V	Negative power supply	30	WIDTH	Test point for Start-Stop duration

FUNCTIONAL DESCRIPTION:

TAC HYBRID is available in 30 pin version as shown in pin diagram and mechanical details.
Stop input is NIM pulse, which is converted into ECL internally.
Start input is ECL negative pulse. The time between Start and Stop generates gate width of time, which is the time between start and stop.

Initially, reset is applied and the circuit is continuously kept in this state. The reset of the hybrid & start can be tied together. The high state of start & reset ensures that internal transistor and the DMOS switch is in ON state and keeping the capacitor C1 at a constant internal reference voltage of 5Vand can be adjusted by external resistors i.e. R-FB and R-IN. When the start (ECL logic) goes to –1.6v i.e. falling edge (low state) the switch turns off, and, the capacitor C1 discharges through constant current source. The discharge current is controlled by the current source at the tail of transistor and external resistor (R-current) can adjust this current to full scale.

Now when Stop comes, this is a fast NIM pulse, the stop latch gets set. The voltage on the capacitor remains constant. The differential amplifier gives an inverted pulse starting from zero with a value (5V-discharge voltage). The settling time of the output is more 200-600ns depending upon the type of the Op-amp.

Now when the Start goes low the circuit is again reset state to begin a new cycle. The output voltage goes to zero.

TPWIDTH : This is test point provided to see the width at the output i.e. time set by the user. User can observe the set time between Start and Stop.

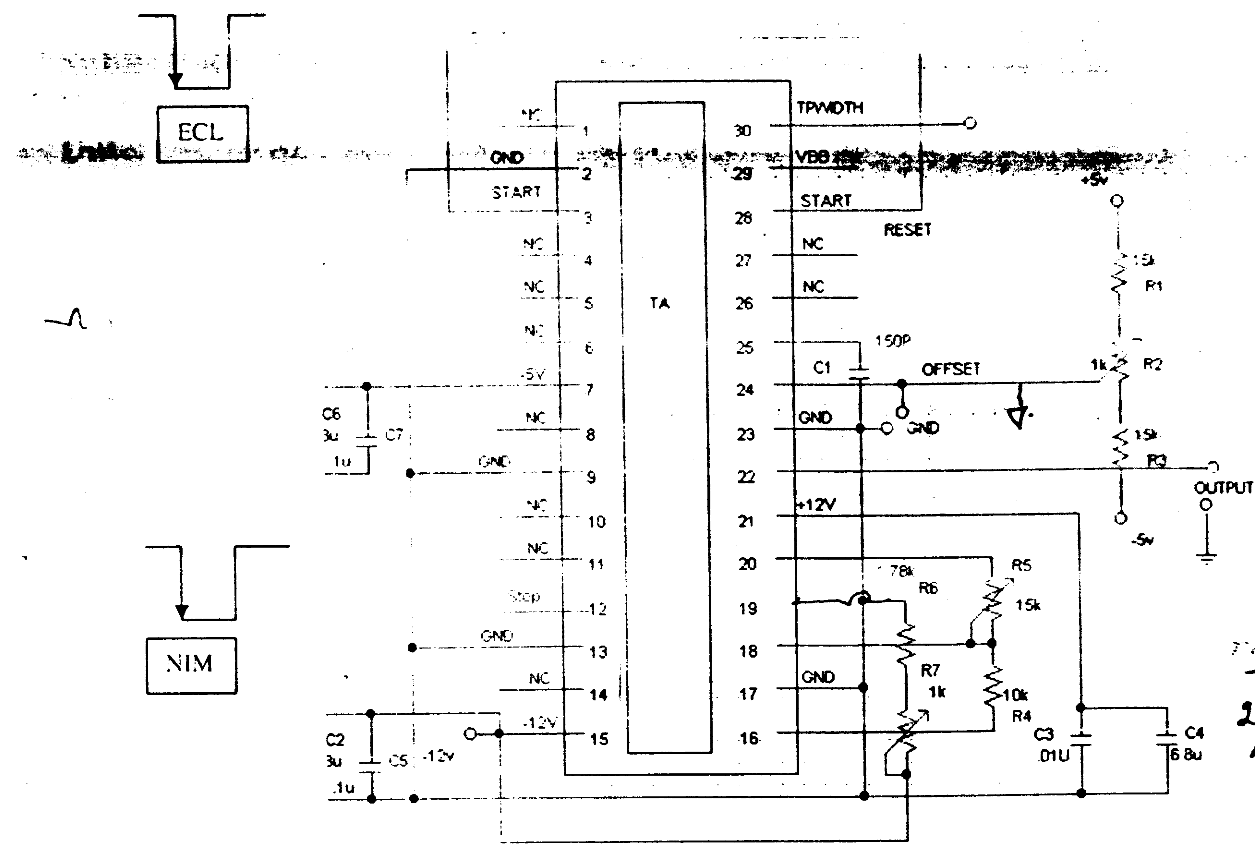
OFFSET: This pin is used to set the output offset at the output pin which will start from zero.

VBB: This is –1.1V input require to set differential pair internally to rest the DMOS Switch.

R_CURRENT: External resistor for full scale adjustment of time correspond to the width i.e. Time between Start and Stop.

CAP : This is the timing capacitor, which can be fixed to any value and then R_Current resistor can be adjusted to required slope.

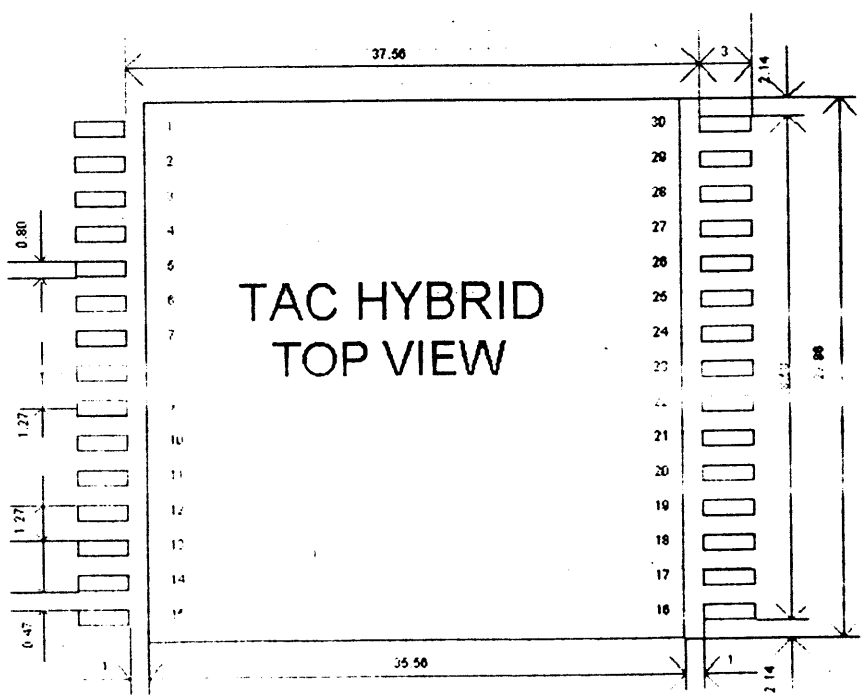
TYPICAL APPLICATION:



$2/47$pF ~ 100ns
+5v
180pF ~ 500ns
82pF ~ 200ns

Ac from
Pin: 20
To extend
o/p range

MECHANICAL DETAILS



Development of Time to Amplitude Converter (TAC) Hybrid

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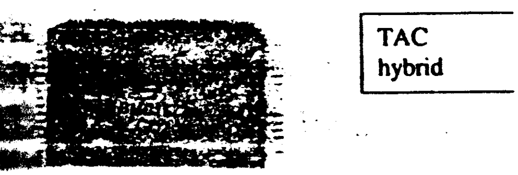
* Correspondence author

Abstract

This paper describes the design and development of a Time to Amplitude Converter (TAC) hybrid. The hybrid features Start, Stop with reset capability and it gives analog voltage ramp proportional to the time interval of start-stop. The hybrid has been designed for 250 ps resolution with Full scale of 500ns. The hybrid is designed, simulated, tested. It was fabricated at BEL ltd using thin film resistors, and dies of semiconductor devices. The hybrid has applications in timing spectroscopy and in instrumentation that demands precise time measurement viz. range finder, echo measurement, etc.

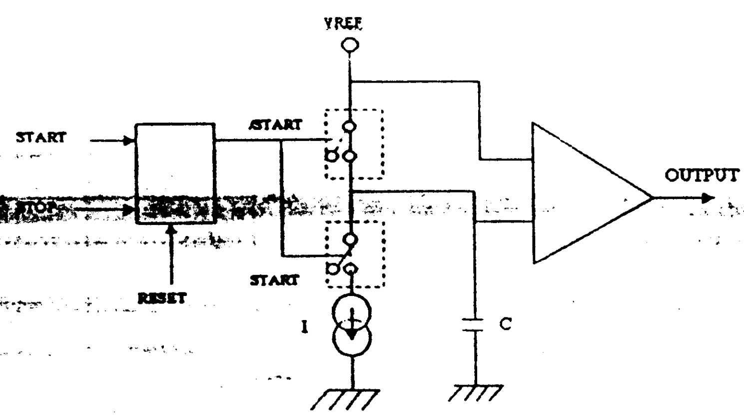
Introduction

There was need to develop a versatile TAC hybrid based on proven designs. The digitization of the TAC ramp output could be done used with Successive approximation ADC or can be interfaced to single slope Wilkinson ADC using a single external current source. This approach would allow higher channel capacity, ease in testing/ maintenance, improving the performance that is critically dependent on layout. TDC is critical component in setups for lifetime measurements in florescence experiments, Time of flight in nuclear experiments, and finds use in laser range finder instruments just to mention critical demanding applications.



Circuit Description

The TAC gives analog output voltages proportional to time between start and stop pulse. Refer to block diagram of the TAC. A Capacitor is discharged by constant current source initiated by START pulse. On arrival of NIM STOP pulse within the full scale, it stops discharging ramp. The difference between the initial and final voltage is

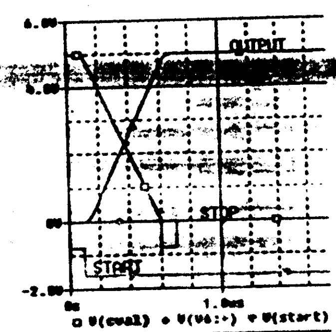


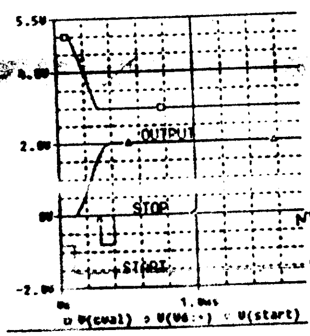
proportional to the time between start and stop pulse. In the existing scheme during the quiescent state the capacitor is held at precise voltage reference Vref. The digital conversion of the TAC voltage can be done by charging the capacitor with a low value of current source and running a clock between stop and capacitor voltage reaching Vref. Other straight forward method is to digitize the voltage using an ADC after 400ns after the stop (settling time of the TAC to final voltage).

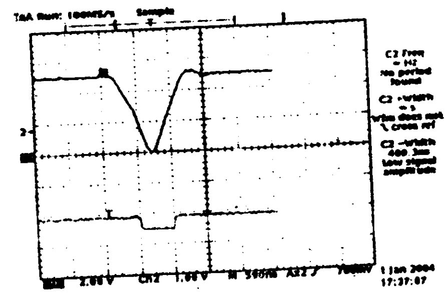
There are three key blocks in this hybrid 1. The Start, Stop, Reset Flip-Flop block 2. The Current source, Voltage reference, ultra fast MOS switch and its driver and 3.The capacitor voltage buffer and the final differential output buffer. Please refer circuit diagram, the Start pulse is NIM level, Stop is ECL level, Reset is ECL/TTL level. The Start pulse is converted to ECL by Q1. MC10102 ECL or/nor gate IC is used as a start-Stop latch. Reset can be connected to Start or it can be external. Constant current source is designed up by using U2A (TL084) quad op-amp and U3 precision LM136 temperature compensated zener diode and J1, Q2, Q3. The reference voltage Vref is generated by using Zener diode and U2B(TL084) Op-amp. This reference voltage can be changed from 3V to 6V. U4 (SD5000) acts like a ultra fast DMOS switch (Ton, Toff ≅ 500ps). The DMOS SD5000 gate voltage driver is designed using differential transistor pair Q4 and Q5. It accepts ECL/TTL reset pulse and gives 0 to 12V fast pulse. The gate overdrive is necessary to make SD5000 switch work as a fast switch. Output buffer is TL084 is used as a voltage buffer for the charging capacitor. It is followed by and differential amplifier that gives the difference between voltage on the capacitor & Vref. This is the TAC Output that settles after 400ns. The charging capacitor is chosen polystyrene or NPO silver mica capacitor due to low dielectric absorption and is critical in TDC.

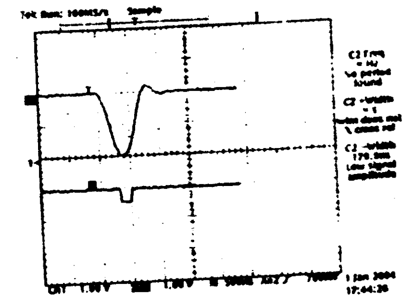
In quiescent state the start-stop latch is in reset state. The switch U4A is closed and the charging capacitor (Cval) is at Vref, also Q5 is on &Q7 is off. The resistance R14,R13, R23,R24 are used as level translators. On the arrival of start U4A opens and Q7 becomes on and discharges the capacitor from Vref until STOP arrives. At stop Q7 goes off. The voltage on the capacitor is buffered by U2C. U2 is a FET input op-amp. The final output is taken as differential of Vref & Vcal.

The entire design was simulated in PSPICE A/D. The design worked as simulated in the very first iteration of fabrication, done at BEL ltd. The resistor R28 is physically absent and









is used for simulation to overcome convergence problems in the simulator due to the DMOS switch. The results of simulation are shown below for 500ns & 200ns start stop interval.

Testing

The TAC is tested for analog output for different values of time interval using DG535 Digital delay generator and using cable delay. TAC hybrid is giving linear output, which is observed on the oscilloscope. Observed outputs on oscilloscope are matching with simulated output. The range of full scale can be increased/decreased by changing the value of external resistor. The Observed out put is shown below.

Key Specification

Start	: ECL
Stop	: Fast NIM
Reset	: TTL /ECL
Output Full scale voltage	: 0 to +5V
Range: min -max	: 500ns
Power Supplies	: ±12v,-5.3V
Power consumption	: Less than 500 mWatt.
Package	: DIP 30.

Conclusion

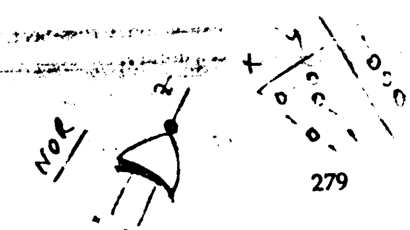
The performance of the circuit is tested on test board. The design of 12 bit ADC interface to digitize the TAC output is underway. A CAMAC module is designed. The performance of the TDC is expected as design as the hybrid is natural progress of existing TDC module further the hybrid offers ease of testing & maintainability of TAC modules. The TAC hybrid is available for as off-the-shelf component from BEL or BARC.

Acknowledgement

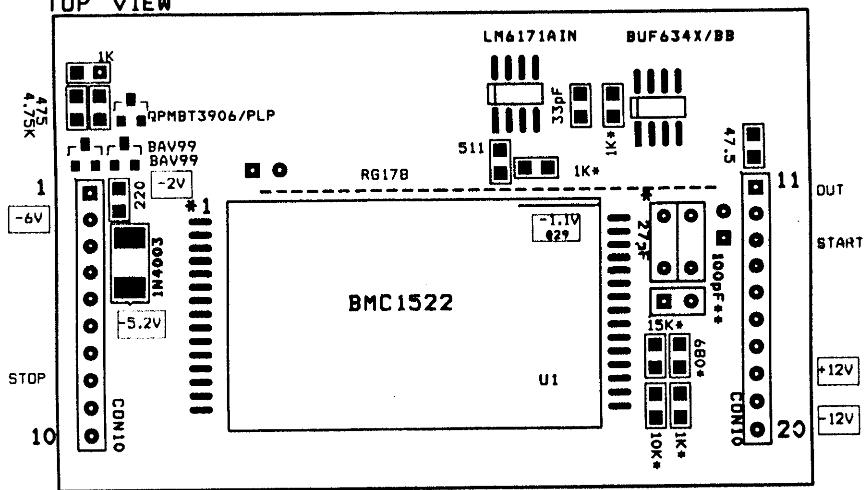
We are thankful the support & encouragement provided by G Govindrajan Director E& I and A&M. We wish to record out sincere appreciation to Mr Parekh of M/S Electron for all the PCB error free design services he rendered that is always of excellent quality.

Reference

1. "CAMAC octal TDC " V.B.Chandrate, R.S.Kapatral, M.D.Ghodgaonkar, K.R.Gopalkrishanan. SANAI-97 p 70.

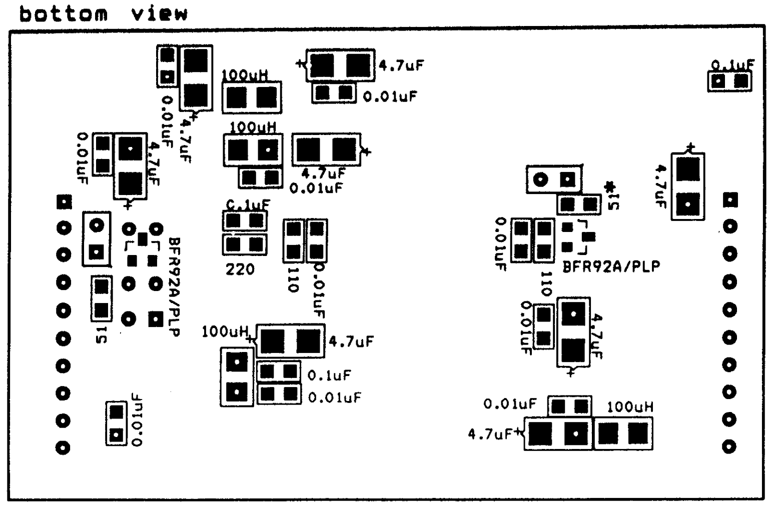


TOP VIEW * OPTIONAL



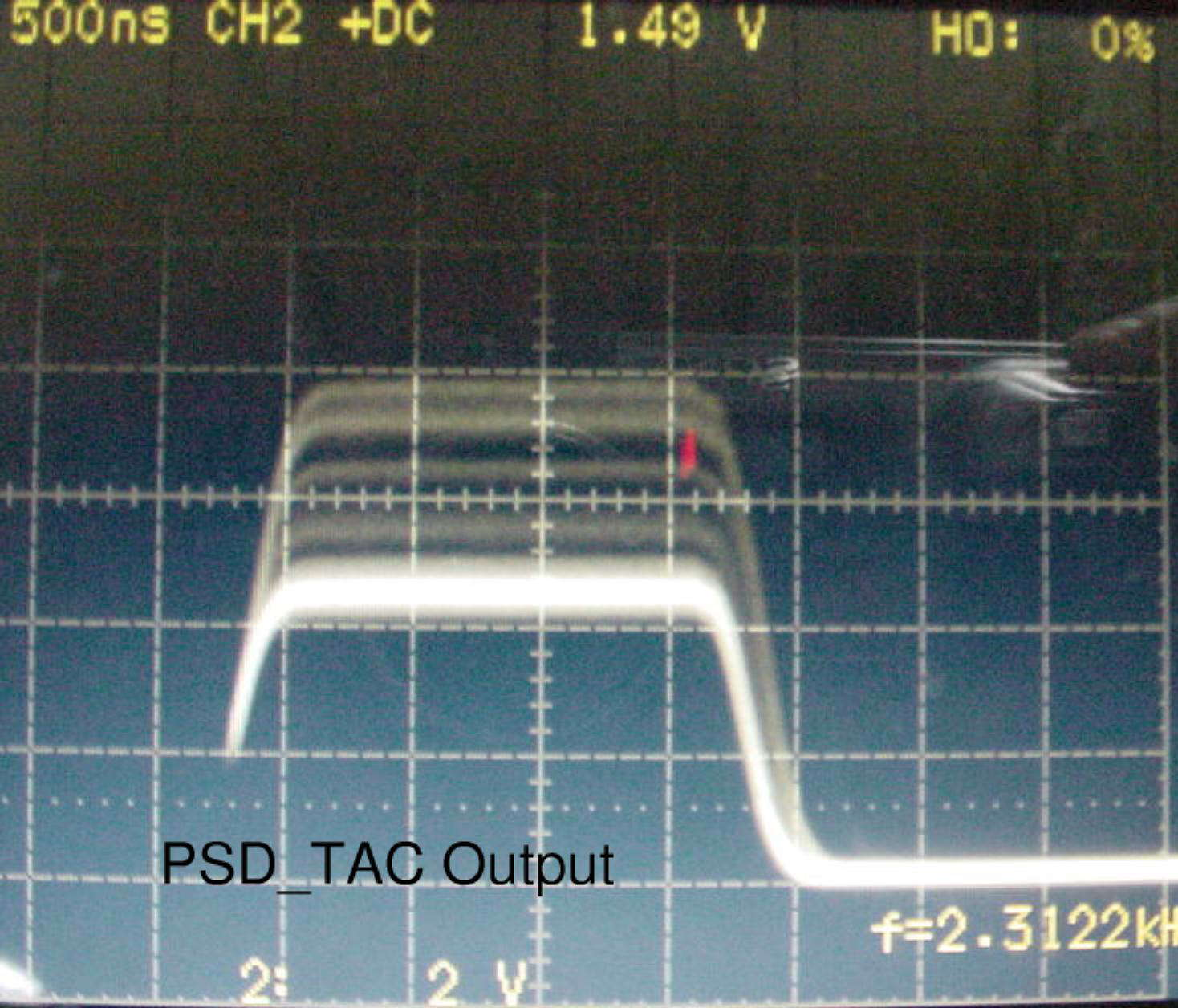
* 25PPm, 1% MFR 15K* = 10K +5.1K
** optional for other ranges

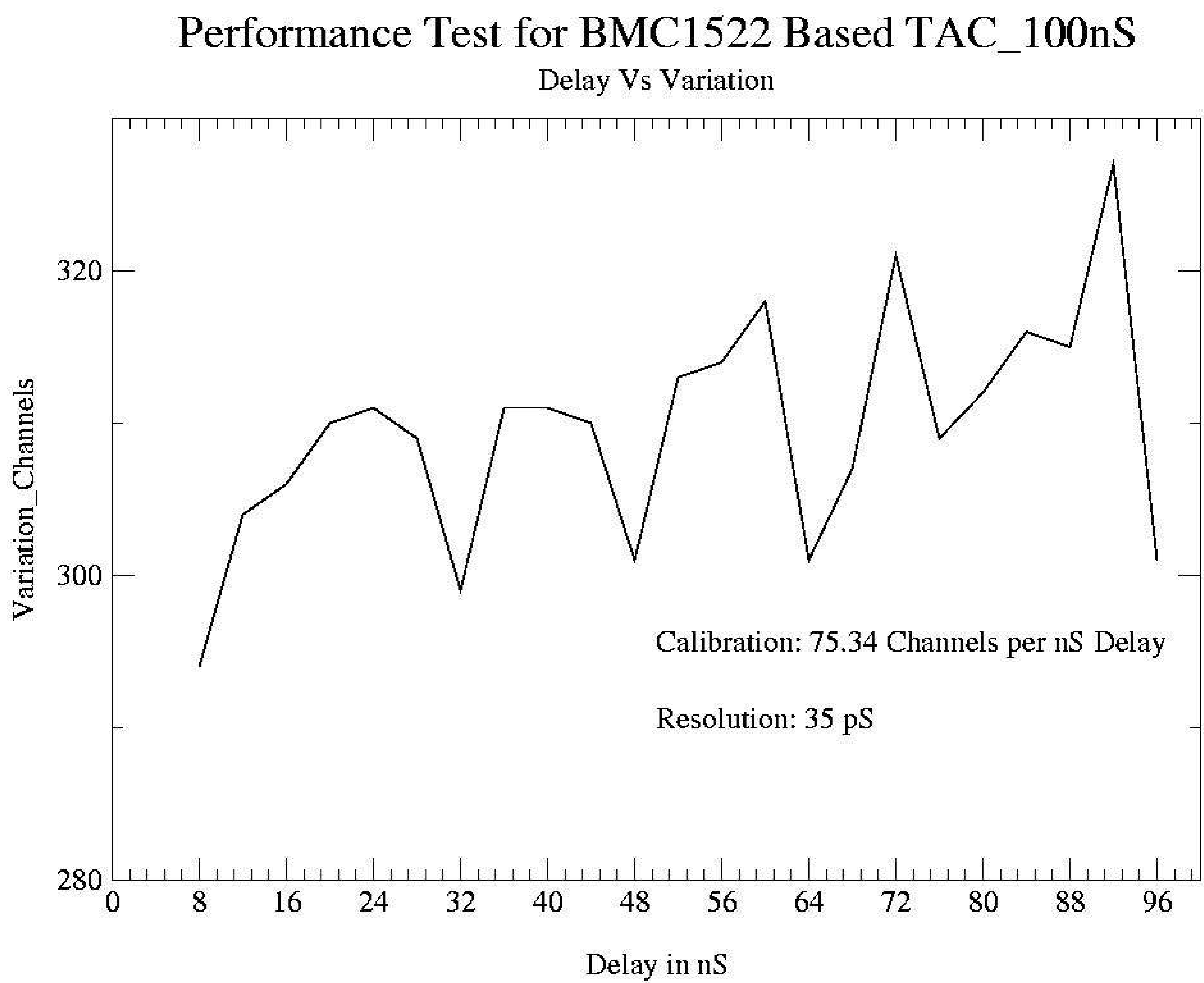
bottom view



TANTALUM TYPE CAPS: 20V
* optional/ not required


TAC_PT3
ELAB/IUAC
08/2005
BMC1522
A09
R14
Q3
M1.1
D2
D1
M2V
J2
R13
D3
U2
R10
C1
R1
BBBUF
634U
9716
U3
R9
WIDTH
C2 C3
J3
R4 R2
R5 R3


500ns CH2 +DC 1.49 V HO: 0%
PSD_TAC Output
f=2.3122kH
2: 2 V


Performance Test for BMC1522 Based TAC_100nS
Delay Vs Variation
Variation_Channels
320
300
280
0
8
16
24
32
40
48
56
64
72
80
88
96
Calibration: 75.34 Channels per nS Delay
Resolution: 35 pS
Delay in nS