TECHNICAL REPORT

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TECHNICAL REPORT ON

CLOVER ELECTRONICS MODULE for INGA

CONTENTS

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TECHNICAL REPORT ON

CLOVER ELECTRONICS MODULE

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Abstract:

A prototype NIM module containing Shaping amplifiers, TFAs, CFDs and logic circuitry for processing signals from a Clover detector with Anti Compton Shield (ACS) has been developed. The circuits are realised in High density daughter card form using SMD components, while keeping the features and specifications at par with commercially available modules. Two numbers of Pre-production modules are assembled and being successfully used with INGA-HIRA experimental setup with particle beam.

Acknowledgment

We would like to thank Engineer and Scientists from GIP, Ganil, France for their constant support in simulating various circuit blocks and for fruitful discussions. Our sincere thanks to Dr.Amit Roy, Prof. G.K.Mehta for their constant encouragement and providing the necessary infrastructure inorder to complete this project successfully. We also thank M/s.ANCOMP for their help in providing good quality PCBs.

Introduction

The experimental facility like INGA consists of a large number of HPGe detectors. Each channel requires a Spectroscopy amplifier, Timing Filter Amplifier (TFA) and Constant Fraction Discriminator (CFD) and associated Logic circuits. Typical commercial electronic setup would require a large number of modules which occupy large area, interconnecting cables and connectors. The NIM module developed at NSC contains five channels of electronics to accommodate one clover with accompanying anti-Compton shield. The content of this double width NIM module is shown in fig 1.

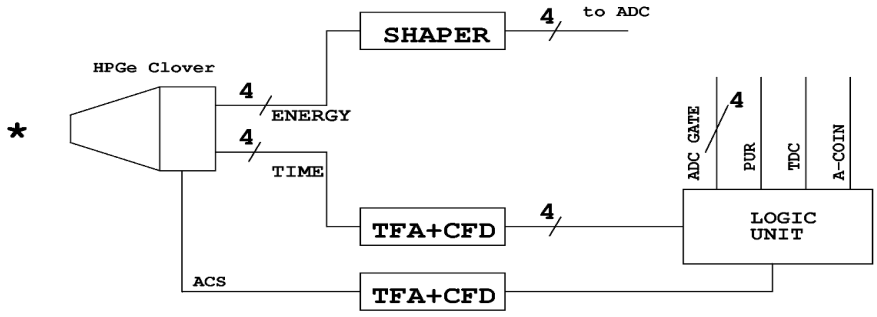


Fig:1 Clover Electronics Bolock Diagram

The high resolution spectroscopy amplifiers have fixed 3μs shaping constant and 3 fixed gain settings (2, 4 & 6 MeV) which are jumper selectable. The DC baseline is stabilized with Gated BLR, while P/Z and BLR (manual) threshold adjustments can be remotely voltage controlled. The unipolar output has the dynamic range of 8 volts across 50 ohms.

Four TFAs with fixed time constants and gain settings are provided for processing TIMING signals from Clover detector. The TFA is designed with single CFA gain stage and baseline is stabilized with twin diode restorer and high input impedence buffer. These amplifiers have rise time of better than 10 ns across their dynamic range of ±2.5 volts across 100 ohms. The CF Discriminator with amplitude & risetime compensation (ARC) is realized with fixed delay of 25 ns and fraction of 0.3. The Lower Level Threshold, WALK adjustment and Monitoring are possible on front panel. The CFD outputs from the individual Clover elements with width of 50 ns and dead time of 2 μs are available internally.

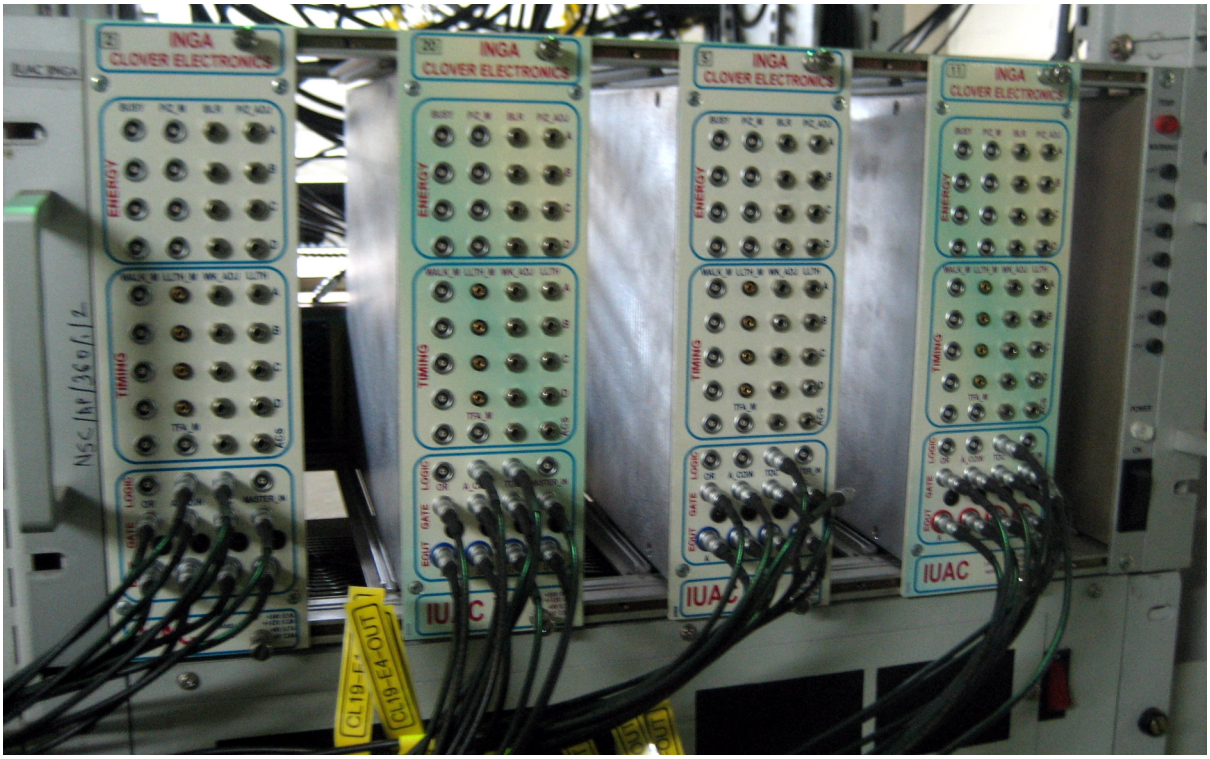
Anti-compton shield signal received from preamplifier is processed with identical TFA + CFD as mentioned above but without dead time. The raw timing logic signals received from CFDs from Clover detector and ACS detector are further processed to affect Anti-coincidence. The TFA and CFD outputs from the ACS are available on the front-panel for ease of adjustment. The logic functions performed are Pileup Rejection, Individual ADC GATing, Anti-Coincidence output and Delayed STOP signal for TDC. All these logic outputs are buffered and available in standard logic levels on the panel.

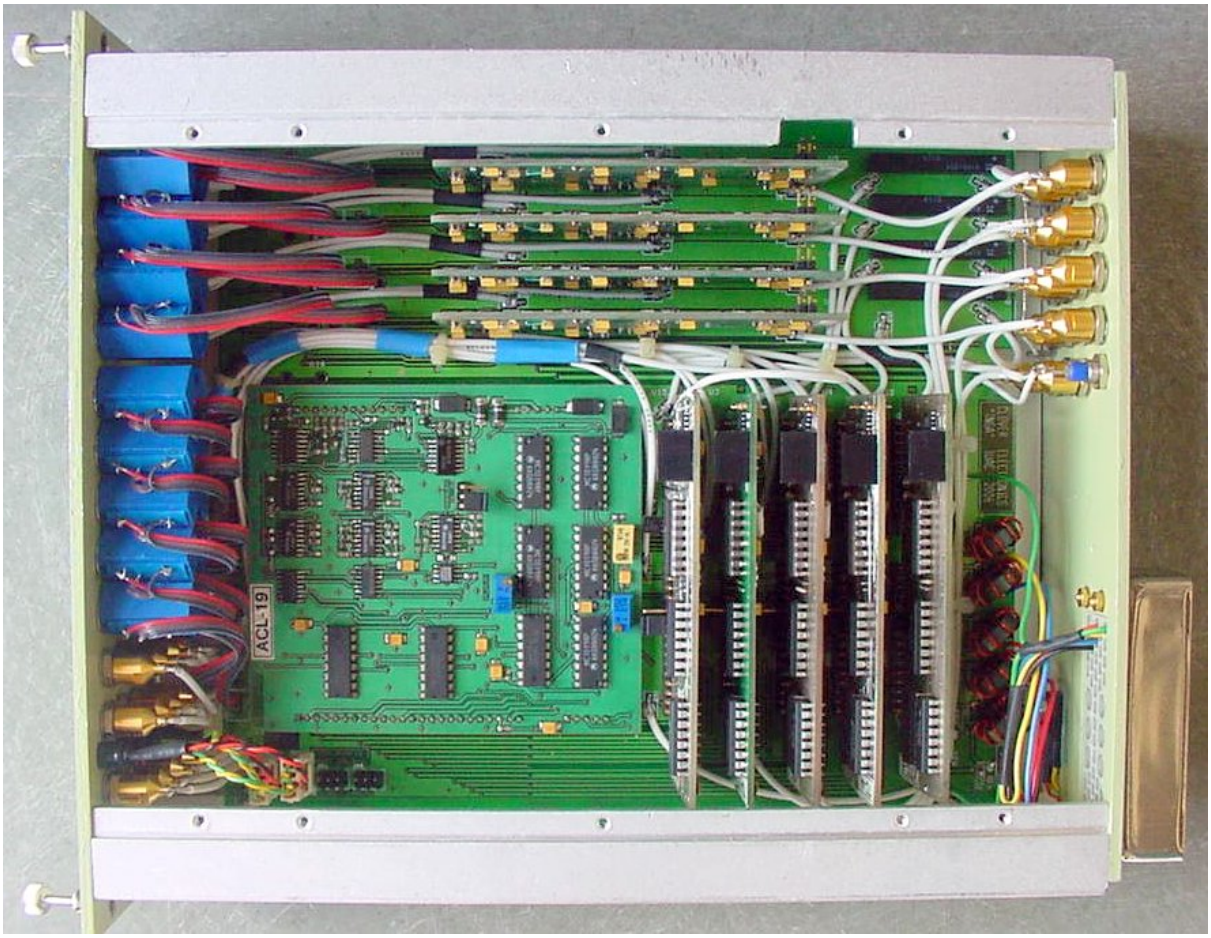
Principle of Operations

The clover Electronics Module essentially contains a mother board where individual blocks in daughter card form are inserted. The rear panel receives the inputs like "ENERGY" and "TIME" signals from Preamplifier through Lemo connectors. The Front panel provides the various monitoring points like P/Z Mon., BUSY, WALK_MON, Energy OUT, ADC GATE and other Logic related signals (TDC STOP, ACOIN..) through Lemo connectors andmanual control of various adjustment like P/Z Adj., BLR Threshold adj., WALK adj., LLTH adj., through multiturn potentiometers. The TFA and CFD outputs corresponding to ACS are provided on front panel for convenience. The panel layout can be seen in attached photograph or drawing.

The high frequency signal layout techniques are widely used for reduction of ground loop related and pick-up problems in the motherboard. RG178C/U coaxial cable is used for interconnection along with ground cap with Lemo-00 series connectors. Typical cable lengths used for various interconnecions inside the moule are listed here. The Timing signals from TFA+CFD block are routed through 100 ohm differential ECL lines for further processing. The detailed operartion priniples of various blocks briefed here can be obtained from individual technical reports prepared by the Electronics Laboratory.

The technical specifications, photographs, representative signals seen on CRO of Shaping Amplifier, TFA+CFD, ACOIN LOGIC UNIT are attached for references.


INGA
CLOVER ELECTRONICS
ENERGY
TIMING
IUAC
CL19-F
CL19-EA-OUT


ACL-19


INGA
CLOVER ELECTRONICS
BUSY
P/Z_M
BLR
P/Z_ADJ
ENERGY
A
B
C
D
WALK_M
LLTH_M
WK_ADJ
LLTH
TIMING
A
B
C
D
TFA_M
ACS
LOGIC
OR
A_COIN
TDC
MASTER_IN
GATE
EOUT
A
B
C
D
IUAC
LABEL
HERE
+24V: 0.1A
+/-12V: 0.3A
+6V: 0.7A
-6V: 2.5A

SPECIFICATIONS
CLOVER ELECTRONICS MODULE @ October 2002

ENERGY

4 SHAPERS with 3μS Shaping constant and fixed gain for
2* MeV/ 4 MeV/ 6 MeV.
* Default selection, Selected with 2 jumpers on PCB.
Input and Outputs are accessed through LEMO connectors on Rear and Front panel respectively.

Controls for P/Z adjustment and BLR Threshold on Front panel.

Monitoring of BUSY and CLAMPED E_OUT (P/Z MON) possible through Front panel LEMO connectors.

TIMING

5 Timing Filter Amplifiers and Constant Fraction Discriminators for 4 clover detectors and ACS respectively.

Timing Inputs are through Rear panel LEMO connectors.

WALK ADJUST, LLTH ADJUST, WALK MONITOR#, LLTH MONITOR on front panel.

TFA (attenuated) and CFD (F_NIM) for ACS is provided on front panel.

#For ACS the "WALK_MON" is available on rear panel.

ANTI-COINCIDENCE LOGIC UNIT

Accepts all required timing informations in ECL complementary logic levels from TFA+CFD units. The outputs and Monitors are provided on front panel through LEMO connectors.

The DELAY and WIDTH adjustments are possible on PCB.

*MASTER GATE (**MGATE_IN**) is TTL logic (positive) with "pull up" resistor.*

POWER SUPPLY The required power supply lines are filtered through 'pi' filters.
A -2Volts supply line for ECL termination is generated in a series pass zener regulator on board.

CABINET Double width NIM module

SPECIFICATIONS SPECTROSCOPY AMPILIFIER*

Input Impedance	~1000 ohm
Pole/Zero adj.	Input pulse having decay time about 50μSec ± 5% can be corrected through potentiometer (FP) or remote controlled through DAC. Input impedance: 1K Control voltage not to exceed ± 1Volt.
Shaping time & type	~3 μSec. Fixed, Active integration (4^{th} order) Quasi Gaussian having peaking time of 2.4τs.
Input signal*	-200mV/MeV is expected to generate +10 Volts at the output for 3 gain settings. Not to exceed ±10V.
Gain	2MeV, 4MeV and 6 MeV for +10V output. Jumper selection on board. Default is 2 MeV.
BLR threshold	Manual baseline restorer threshold is set through Potentiometer(FP) or remotely. Range is 0 to 300mV when provided. Impedance is 1k. Control voltage not to exceed ±10V
Output	Unipolar, Gated BLR DC restored. Width :~20μSec. Impedance 50 ohm
BUSY	A TTL negative logic pulse for the duration of presence of output pulse exceeds BLR threshold. Impedance: 10 ohm.
PUR	Pile up reject signal is a TTL positive logic signal, with pileup inspection interval of 20μSec. Impedance: 10 ohms.
Power required*	+/-6V, 40mA/20mA +/-12V 40mA/30mA +24V 5mA
Size & Weight	W x H x L : 1.75"x0.5"x 4", 30 grams.
Technology	Double sided PCB with PTH and SMD components are used.

PERFORMANCES:

The module has been subjected to various tests at NSC with ^{60}Co and ^{152}Eu sources and in beam, in parallel with commercial modules. The typical results obtained are :

Resolution: **1.3KeV (122KeV), 2.0 KeV (1408 KeV) of ^{152}Eu @ 9 Kcps.**

Integral non-linearity: **± 80 eV for ^{60}Co spectrum**.

Stability: **With ^{60}Co, no significant shift observed at 6 kcps in 55 hours.**

SPECIFICATIONS:	**TIMING FILTER AMPILIFIER***
INPUT IMPEDANCE	50 ohms.
GAIN(fixed)*	~10 The input of -200mV/MeV is expected from Preamplifier.
OUTPUT AMPLITUDE	0 to ±2.5V into 50 ohm cable and load.
OUTPUT IMPEDANCE	~1 Ohm
RISE TIME	Better than 10nSec. With no additional integration across dynamic range.
STABILITY (DC)	Twin diode restorer used.
POLE/ZERO ADJ.*	P/Z internally corrected for 50μS (±5%) decay time internally.
DIFFERENTIATION	200nS (C1 X R12)
INTEGRATION	none. (R4 X Cx)

* For ACS, the P/Z network is wired for 400nS internally to match the decay time of BGO phosphor.

SPECIFICATIONS: CONSTANT FRACTION DISCRIMINATOR*

INPUT SIGNAL	Negative pulses accepted upto -5V
THRESHOLD RANGE (LLTH)	+60mV to -200mV Front panel adjustable.
LLTH MONitor	Measures x10 of actual LLTH set value.
DELAY	Internal, Zo = 100 0hm, 25nSec Fixed.
FRACTION RATIO	x 0.3
WALK ADJUST	Front panel control for exact zero-cross voltage.
WALK MONitor	Front panel LEMO connector for monitoring CF signal.
DEAD TIME	2 μS. (Fixed)
WIDTH	50nS.(Fixed)
OUTPUTS	ECL DIFFERENTIAL 2 μS ECL DIFFERENTIAL 50 nS. FAST NIM (2 nos.) 50 nS.
IMPEDANCE	100 ohm DIFFERENTIAL ECL 50 ohm FAST NIM
OTHERS	SRT/CFD selection (Jumper on board)
DIMENSION (WXHXL) & WEIGHT	1.5" x 4" x 0.5", 50 grams
TECHNOLOGY	Both SMD and Through hole components used. PCB Double sided with PTH.

Note: For ACS, the same CFD daughter card is utilized without any dead time and output having width of 500 ηS.

SPECIFICATIONS: ANTI_COINCIDENCE LOGIC UNIT*

INPUTS (Internal) ECL COMPLIMENTARY

CHANNEL A	CFD 2 μS DEAD TIME CFD 50 nS. width
CHANNEL B	CFD 2 μS DEAD TIME CFD 50 nS. width
CHANNEL C	CFD 2 μS DEAD TIME CFD 50 nS. width
CHANNEL D	CFD 2 μS DEAD TIME CFD 50 nS width
AC SHIELD	CFD 500 nS width

MASTER GATE (MGATE_IN)
TTL (positive) internally pulled up input.
Must arrive within 1μS of individual CFD outputs.

OUTPUTS

ANTI-COINCIDENCE (A_COIN)
FAST NIM (Front panel LEMO)
WIDTH 500 nS. (adjust on BOARD)
After "OR"ing of CFD (50 ns) outputs from channels A to D "DELAY"ed by ~100 nS. GATED with ACS (500 nS) for Coincidence and output is generated.

START/STOP (TDC)
FAST NIM (Front panel LEMO)
WIDTH 50 nS
After Coincidence, the signal is DELAYED (200 nS-800 nS Adjusted on BOARD) and output is generated.

MONITOR (OR_P)
FAST NIM (Front panel LEMO)
WIDTH 100 nS
The CFD (50 nS) outputs are logic ORed and and delayed ~100 nS

ADC GATEs (GATE A-D)
Positive TTL (Front panel LEMO)
Zo: 10 ohms.
WIDTH 10 μS. Refer to Block diagram. Generated only when Master_Gate is present with 1μS of the input signal.

PUR SUM (PUR A-D)
POSITIVE TTL (Rear panel LEMO)
PUR inspection WIDTH 20 μS
Zo: 10 ohms. It is "OR" of four piled up channels.

DIMENSION
4 " x 0.5" x 3.75" 80 grams. W x H x L

NOTE: * Refer individual technical report for details.

Schematic Diagram

For easy references, a set of circuit diagrams are attached. The circuit diagram of individual blocks are given alongwith. The entire mother board is mounted on side rails of a double width NIM module. The individual blocks are assembled in daughter card form and plugged into low profile machine trimmed sockets. The front panel trimmer potentiometers (3006P) are hood mounted. The series pass regulator transistor is electrically isolated and mounted on rear panel for heatsinking.

Assembly Procedure

The currently (MOTHERBRD_PT2, OCT_2002) available PCB is of glass epoxy, double sided with 0.6mm drill PTH having dimension of 7.25" x 8.5". It is recommended to have solder mask and silk screen printed on both sides for easy assembly as well to protect it from solder bridges etc.,. Use of 0.2mm sharp solder tip, IC solder tips are recommended in order to solder narrowly spaced SMT devices. SMT devices shall be picked only by fine quality tweezers. While soldering a magnifier x5 (large) and x12 (eye piece) is used to assure the soldering. It is essential to use solder cleaning liquid with cotton swab to remove dust attracting solder paste. The PCB shall be checked with magnifiers and multimeter for any unwanted connections and PTHs. Then components shall be soldered in a orderly manner, to start with all low profile chip resistors and capacitors. It is essential to check the impedance between various nodes after soldering resistors, capacitors and inductors. Active components like diodes, transistors and ICS are soldered thereafter. At last tantalum capacitors, connectors, jumpers and any non-SMT devices. All PCBs shall be marked distinctly with unique number for any future references. The Series pass transistor is mounted in conventional way with heatsink kit.

Reference:

1. Electronics for INGA at NSC by Dr.R.K.Bhowmik

Cable : RG178B/U, Make: BELDEN
Use sharp Industrial knife cautiously to remove sleeve
Use scissors/cutter to remove braid.

Standard lengths to be cut as per this table.

NAME		LENGTH Inches	NAME	LENGTH Inches
FRONT PANEL CONNECTIONS				
PUR		8	BUSY_A	7
A_COIN		7.5	BUSY_B	7
OR_MON		7	BUSY_C	7
TDC		7	BUSY_D	7
MASTER_GATE		7		
GATE_A		7	P/Z_MON_A	5.5
GATE_B		7	P/Z_MON_B	5.5
GATE_C		7	P/Z_MON_C	5.5
GATE_D		7	P/Z_MON_D	5.5
EOUT_A		12		
EOUT_B		12	ACS_CFD	8
EOUT_C		12	ACS_TFA	12
EOUT_D		12		
			WALK_MON_A	9
			WALK_MON_B	9.5
			WALK_MON_C	10
			WALK_MON_D	10.5
REAR PANEL CONNECTIONS				
EIN_A		3		
EIN_B		3		
EIN_C		3		
EIN_D		3		
TIME_IN A		5		
TIME_IN B		4.5		
TIME_IN C		3.5		
TIME_IN D		3		
ACS_IN		5		
WALK_MON-ACS		8		

Connections for Potentiometers are done through Teflon wires, SWG26, multistrand.

BLR_A	3		LLTH_A	9
BLR_B	3		LLTH_B	9
BLR_C	3		LLTH_C	9
BLR_D	3		LLTH_D	9
			LLTH_ACS	9
P/Z ADJ. A	3		WALK_ADJ. A	2.5
P/Z ADJ. B	3		WALK_ADJ. B	2.5
P/Z ADJ. C	3		WALK_ADJ. C	2.5
P/Z ADJ. D	3		WALK_ADJ. D	2.5
			WALK_ADJ. ACS	2.5

Note: The actual length of cable and wire would be less than mentioned here.
Start the connection from connectors in case of Coaxial cable.
Start the connections form PCB incase of teflon wire.
The coaxial cables are terminated on LEMO-00 series through "Earth Cap".