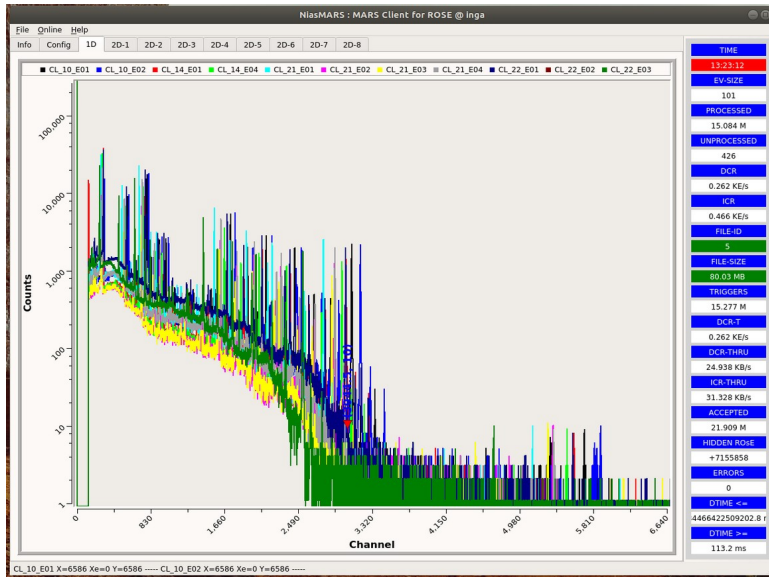
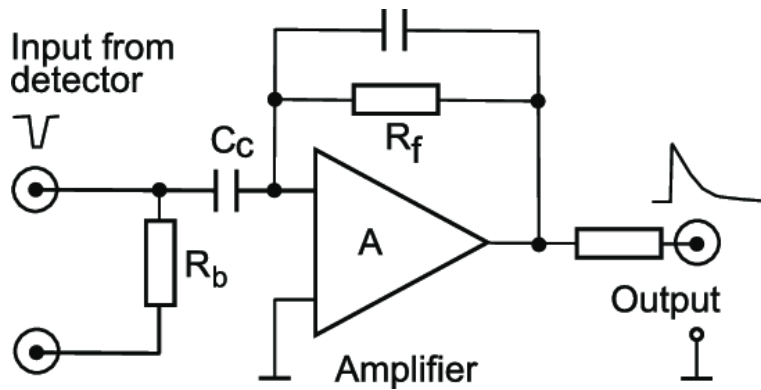


Acquisition, Event of Interest and Timestamp



Components of DAQ

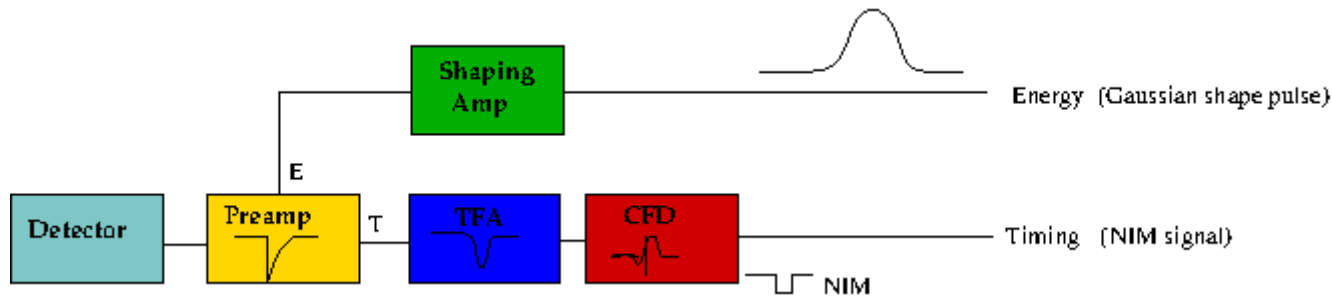


Graphics User Interface/Software

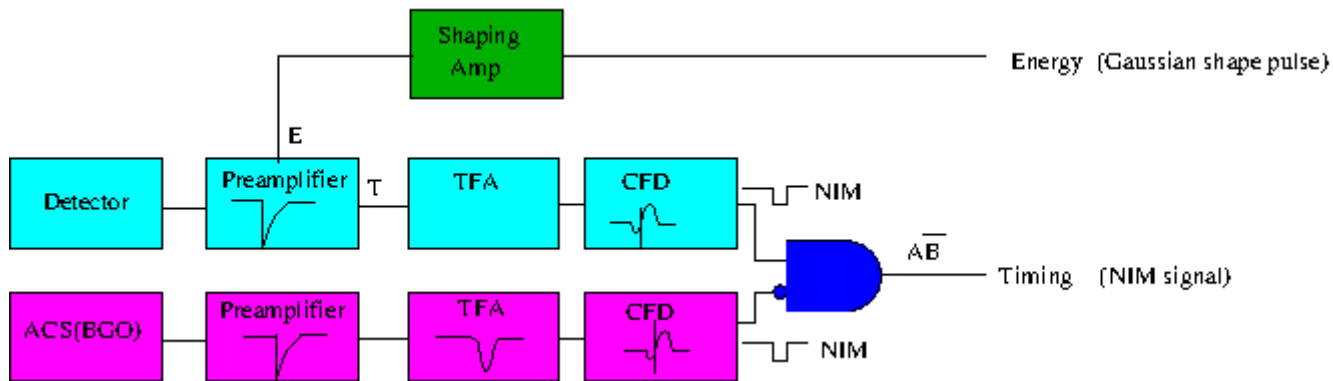
TFA
CFD
Trigger Module
TDC
Shaping Amplifier
ADC
Controller
Computer
Storage.

Back panel or mode of implementation may differ

Event from A detector



Event From HPGe Detector



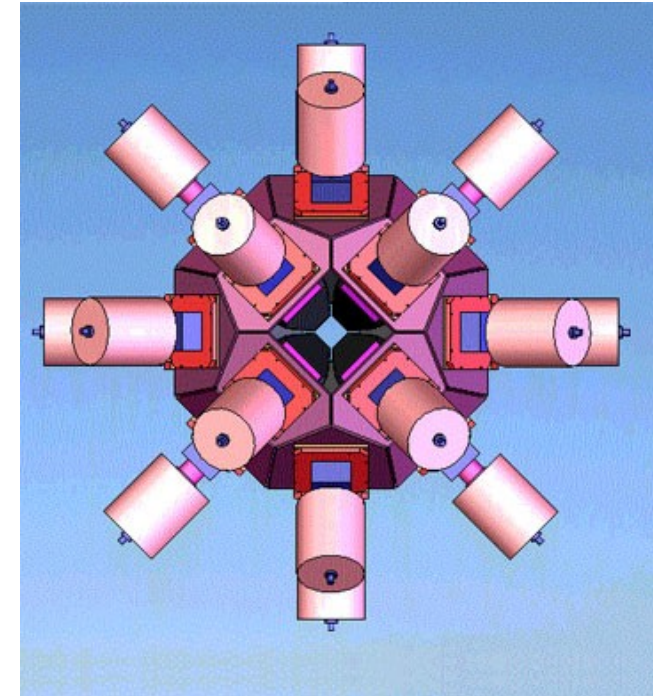
HPGe Detector comes with Anti compton shield to suppress the background noise which is due to Compton scattering.

Compton Scattering ---> partial information

Inhibit the HPGe signal if ACS signal is present.

MODE of Data Collection

Multiple Detector --> multiple signals



Histogram -> No condition for event collection
No Rejection, No Timing correlation

List-mode -> condition apply **
Collected only when a
Events of Interest occurs

What is an Event of Interest (EOI)???

Event which fulfill all the requirement of user and used as a trigger for the DAQ...

User requirements are correlation between the events of the detectors fired with in chosen time frame means range of TDC (400ns/800ns). Basically This is called **Multiplicity**.

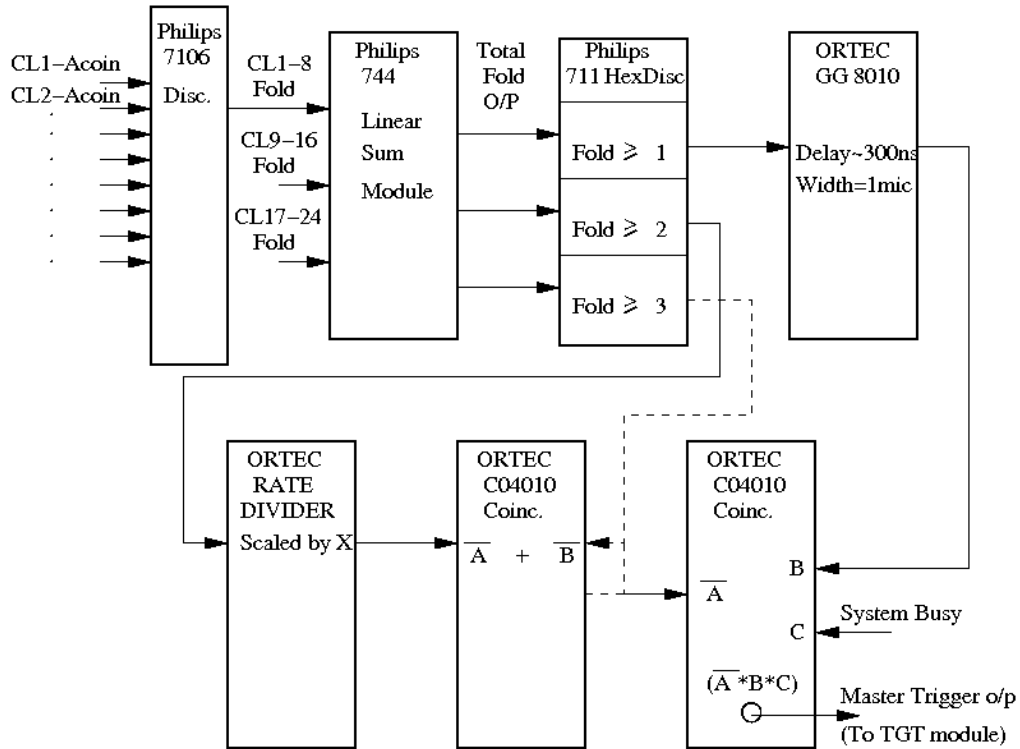
Multiplicity means number of event comes in a given time window....

User can put the conditions :

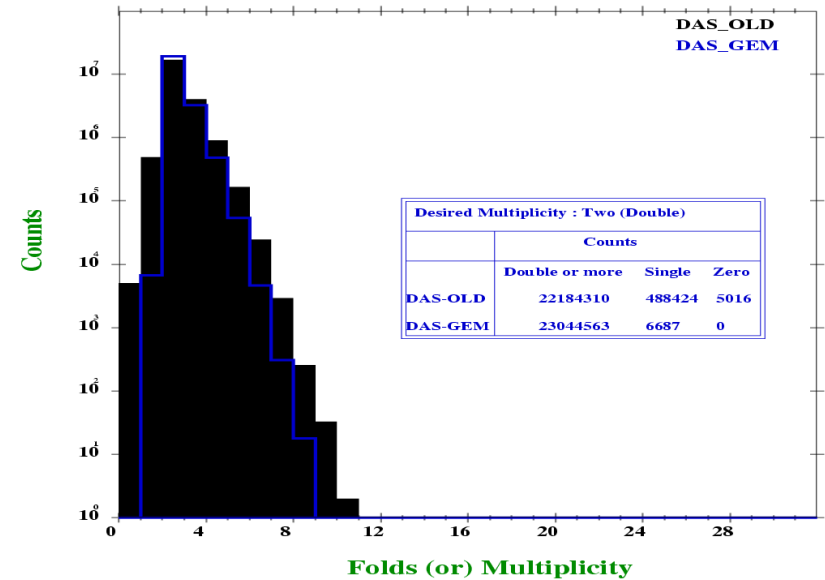
- Collect the data only when the signal comes from at least one detector (1 fold multiplicity)
OR
- Only when the signal comes from at least two detector in a chosen time frame.(2 fold multiplicity)
OR
- Only when the signal comes from at least three detector in sync with some other type of detector in a time window. (3 fold multiplicity)

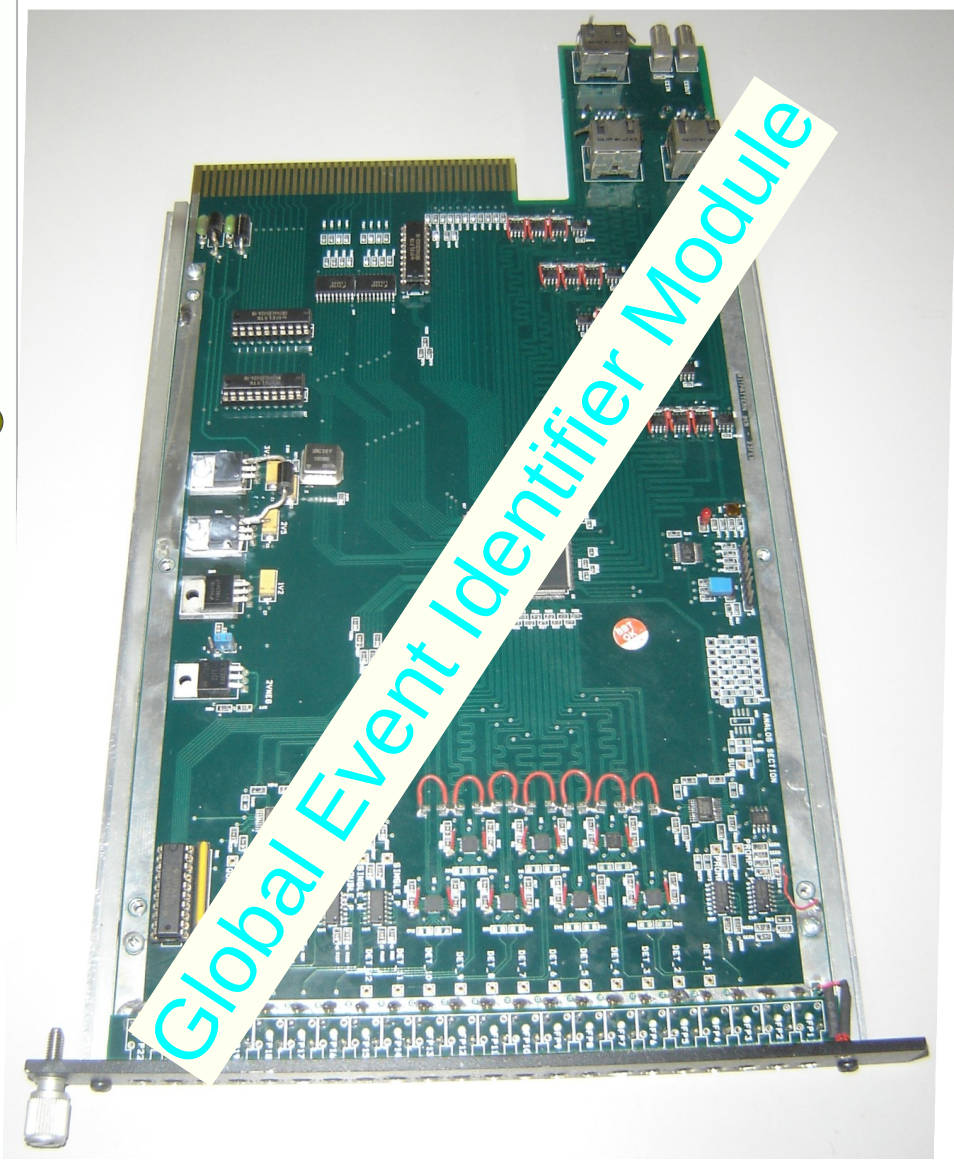
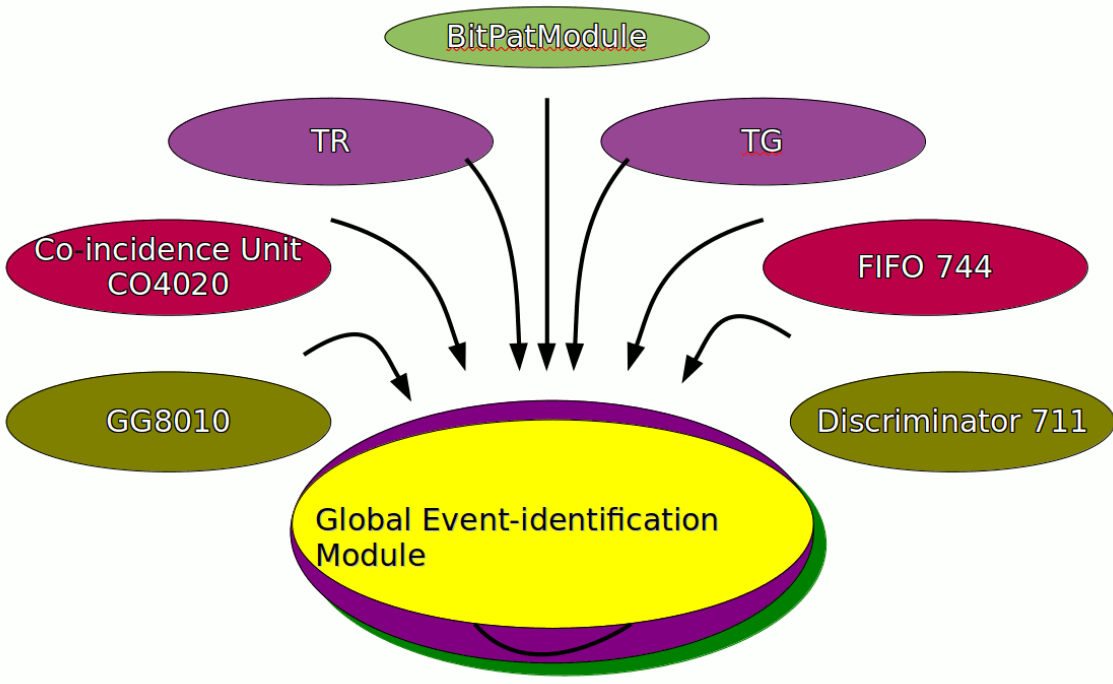
Multiplicity Selection

INGA ELECTRONICS: MASTER TRIGGER LOGIC

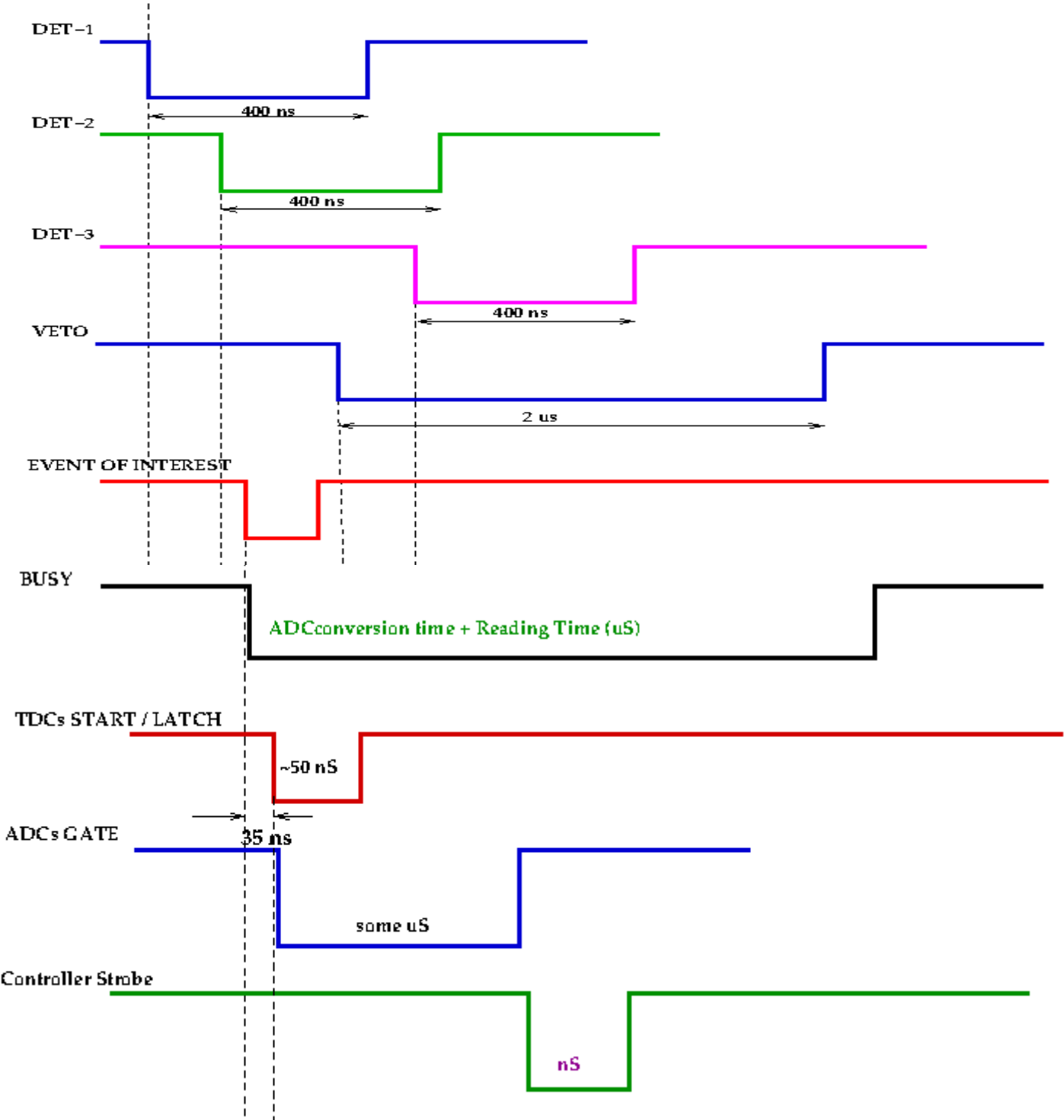


Event-Of-Interest Comparison

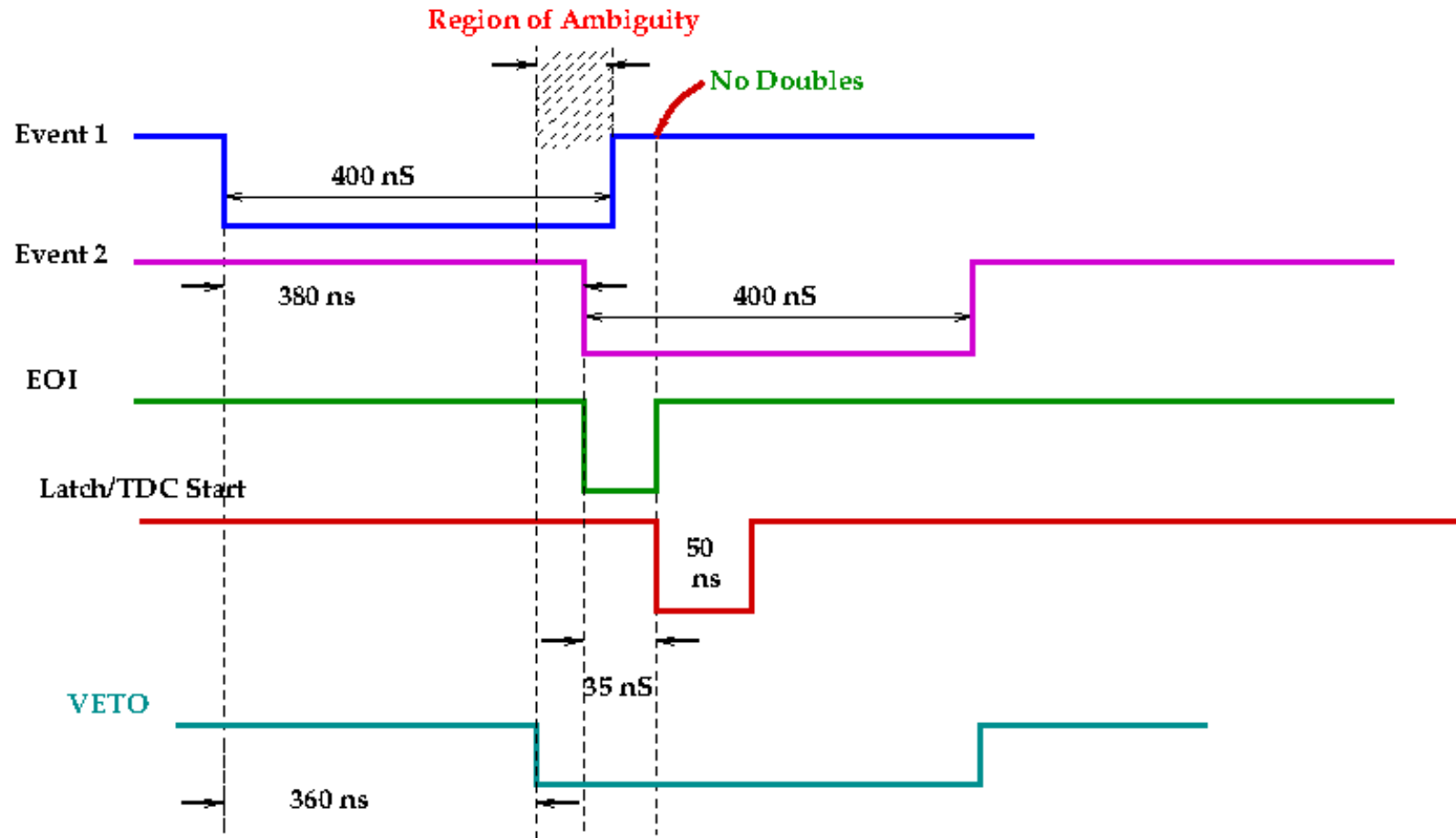




Event of Interest generation (multiplicity -2 fold)



What is VETO ???



In This case Veto is nothing but a delayed signal of singles to prevent the false registration of bit pattern.

How do we implement user requirements ???

Convert them into a logic and write those instructions into the Trigger module through the **Controller**.

Controller ???

Controller is a module which works for us like mediator connected between computer and DATA bus.

List of Command through GUI --> controller --> DAQ Modules

Steps...

- All the event goes to trigger module (GEM) and GEM generate the trigger/Master strobe whenever the user condition satisfied or EOI occurs.
- Also generates a busy signal to block all the incoming event of interest till the system is engage in the processing of Accepted EOI and Time stamp this event along with latching the BIT PATTERN.
- BIT PATTERN contains the information about the fired detector for that particular EOI.
- Every time the Controller gets the trigger, it execute the list of read command which we wrote into the controller memory and send the acquired data to the computer.
- First command in list of controller is BIT PATTERN read.

- Based on the BIT PATTERN information, controller executes remaining command in list. This method is called Zero suppression read.

Zero Suppression READ → Short Read time, less dead time of the system, Space saving

Short Read time, less

INGA ARRAY → 24 Clover → 120 Signals

1 signal ~ 1 uS read time (typically 1.2 uS for one CAMAC cycle)

120 signal → 120uS

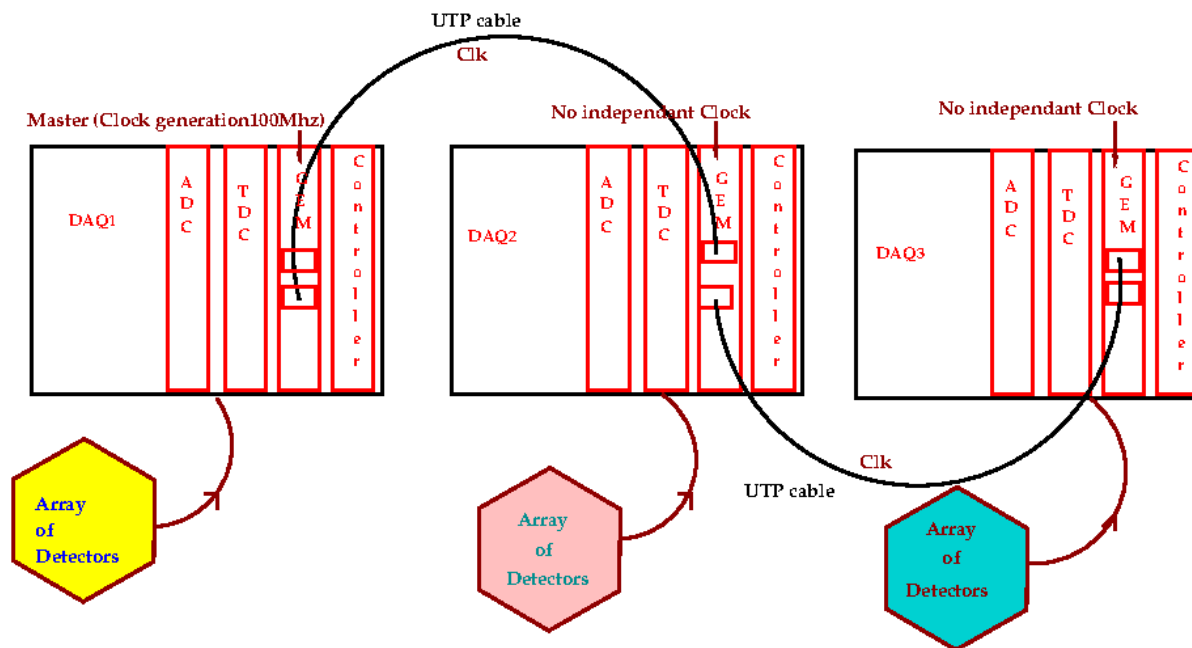
If only 6 detector fired for accepted EOI, in zero suppression technique controller will read only 30 signals. Read time will reduce to 30 uS.



Configuration file for CAMAC

```
Activities Text Editor Feb 24 00:12
*TripleCrate-20181005-24CLOVERS.CAM
My Passport /media/kusum/My Passport/home/kusum/CAM Save
TModule.vhd *TripleCrate-20181005-24CLOVERS.CAM
1 Candle Camac Configuration File
2 USER :Umesh Garg / NDU
3 EXPT :Transverse wobbling
4 BEAM :55 MeV 13C on 94Zr
5 EventsPerBlock=650 EventsToSend=650 CamacMode=Hit Pat Mode
6
7 NumberOfInits=29
8   INPW-0 C=0 N=22 A=1 F=16 DATA=37
9   OUTW-0 C=0 N=22 A=2 F=16 DATA=37
10  LPDLY-0 C=0 N=22 A=3 F=16 DATA=3000
11  VETD-0 C=0 N=22 A=4 F=16 DATA=20
12  VETW-0 C=0 N=22 A=5 F=16 DATA=197
13  ADCW-0 C=0 N=22 A=6 F=16 DATA=2000
14  INPW-1 C=1 N=22 A=1 F=16 DATA=37
15  OUTW-1 C=1 N=22 A=2 F=16 DATA=37
16  LPDLY-1 C=1 N=22 A=3 F=16 DATA=3000
17  ADCW-1 C=1 N=22 A=6 F=16 DATA=2000
18  INPW-1 C=2 N=22 A=1 F=16 DATA=37
19  OUTW-1 C=2 N=22 A=2 F=16 DATA=37
20  LPDLY-1 C=2 N=22 A=3 F=16 DATA=3000
21  ADCW-1 C=2 N=22 A=6 F=16 DATA=2000
22  CDIS-0 C=0 N=22 A=1 F=24 DATA=0
23  CDIS-1 C=1 N=22 A=1 F=24 DATA=0
24  CDIS-1 C=2 N=22 A=1 F=24 DATA=0
25  CCLR-0 C=0 N=22 A=0 F=9 DATA=0
26  CCLR-1 C=1 N=22 A=0 F=9 DATA=0
27  CCLR-1 C=2 N=22 A=0 F=9 DATA=0
28  CLAM-0 C=0 N=22 A=0 F=10 DATA=0
29  CLAM-1 C=1 N=22 A=0 F=10 DATA=0
30  CLAM-1 C=2 N=22 A=0 F=10 DATA=0
31  MULT-0 C=0 N=22 A=7 F=16 DATA=0
32  VETO-0 C=0 N=22 A=8 F=16 DATA=0
33  MasterClk C=0 N=22 A=2 F=17 DATA=3
34  SlaveClk C=1 N=22 A=2 F=17 DATA=0
35  SlaveClk C=2 N=22 A=2 F=17 DATA=4
36  Tsenb C=0 N=22 A=1 F=26 DATA=1
37 NumberOfScalers=0
38 NumberOfSingles=0
39 NumberOfEvents=132
40  Hit-1 C=0 N=22 A=3 F=0 SIZE=255 BITPOS=Always
41  TLO-1 C=0 N=22 A=0 F=0 SIZE=0 BITPOS=Always
42  TMI-1 C=0 N=22 A=1 F=0 SIZE=0 BITPOS=Always
43  THI-1 C=0 N=22 A=2 F=0 SIZE=0 BITPOS=Always
44  CL01-T C=0 N=17 A=0 F=0 SIZE=4095 BITPOS=If Bit Set
45  CL01-E1 C=0 N=2 A=0 F=0 SIZE=16383 BITPOS=If Bit Set
46  CL01-E2 C=0 N=2 A=1 F=0 SIZE=16383 BITPOS=If Bit Set
47  CL01-E3 C=0 N=2 A=2 F=0 SIZE=16383 BITPOS=If Bit Set
48  CL01-E4 C=0 N=2 A=3 F=0 SIZE=16383 BITPOS=If Bit & Inc
49  CL02-T C=0 N=17 A=1 F=0 SIZE=4095 BITPOS=If Bit Set
50  CL02-E1 C=0 N=2 A=4 F=0 SIZE=16383 BITPOS=If Bit Set
51  CL02-E2 C=0 N=2 A=5 F=0 SIZE=16383 BITPOS=If Bit Set
52  CL02-E3 C=0 N=2 A=6 F=0 SIZE=16383 BITPOS=If Bit Set
Plain Text Tab Width: 8 Ln 10, Col 43 INS
```

Stamp the TIME on Accepted EOI



- GEM use 100MHz Clk to time stamp the EOI.
- Module provides a 48 bit time stamp.
- Clk travels in cascaded manners between the distributed DAQs which keeps all the DAQs in synchronization.
- Accepted EOI of distributed system can be correlated later in the analysis.

THANX.....

24 Feb 2023